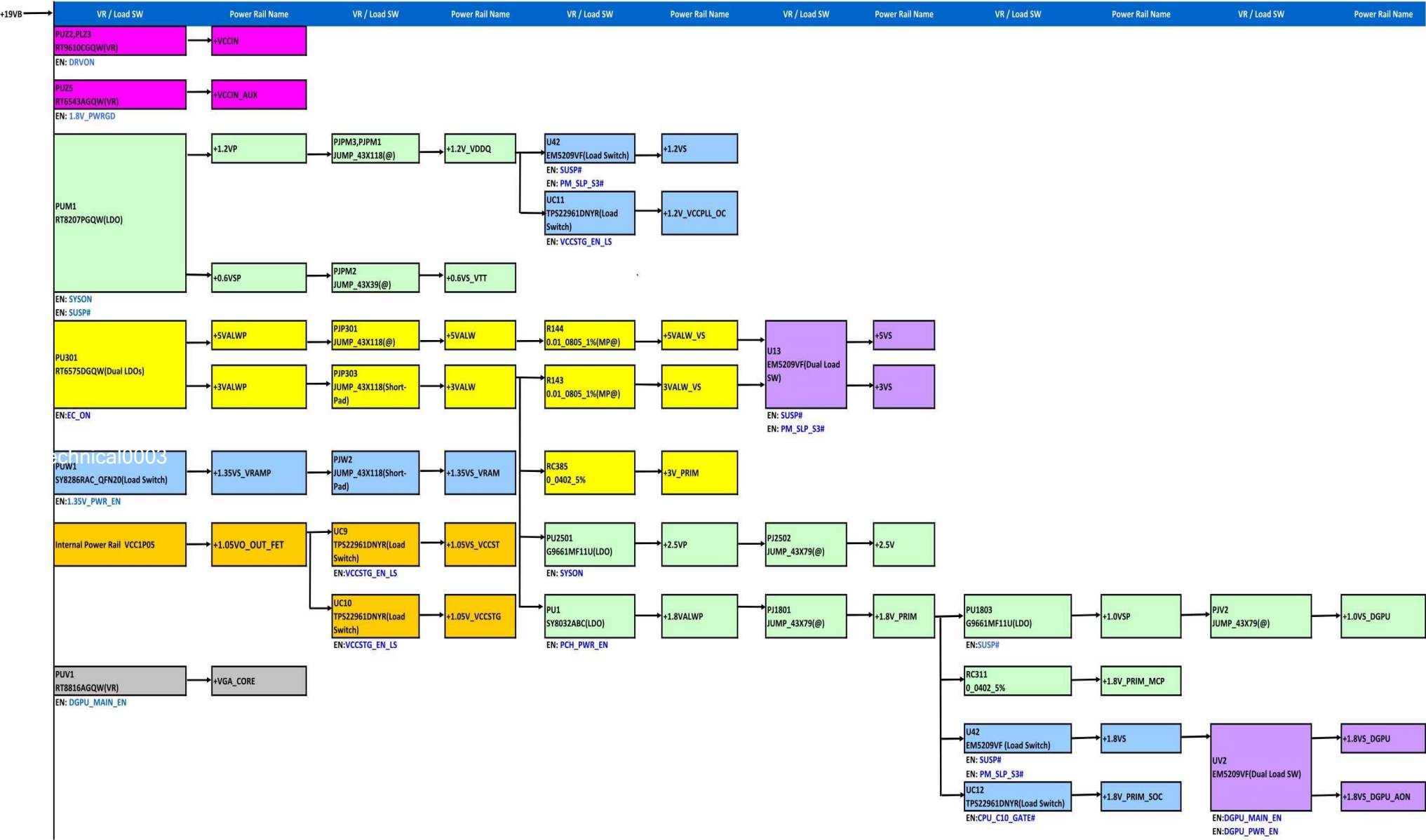
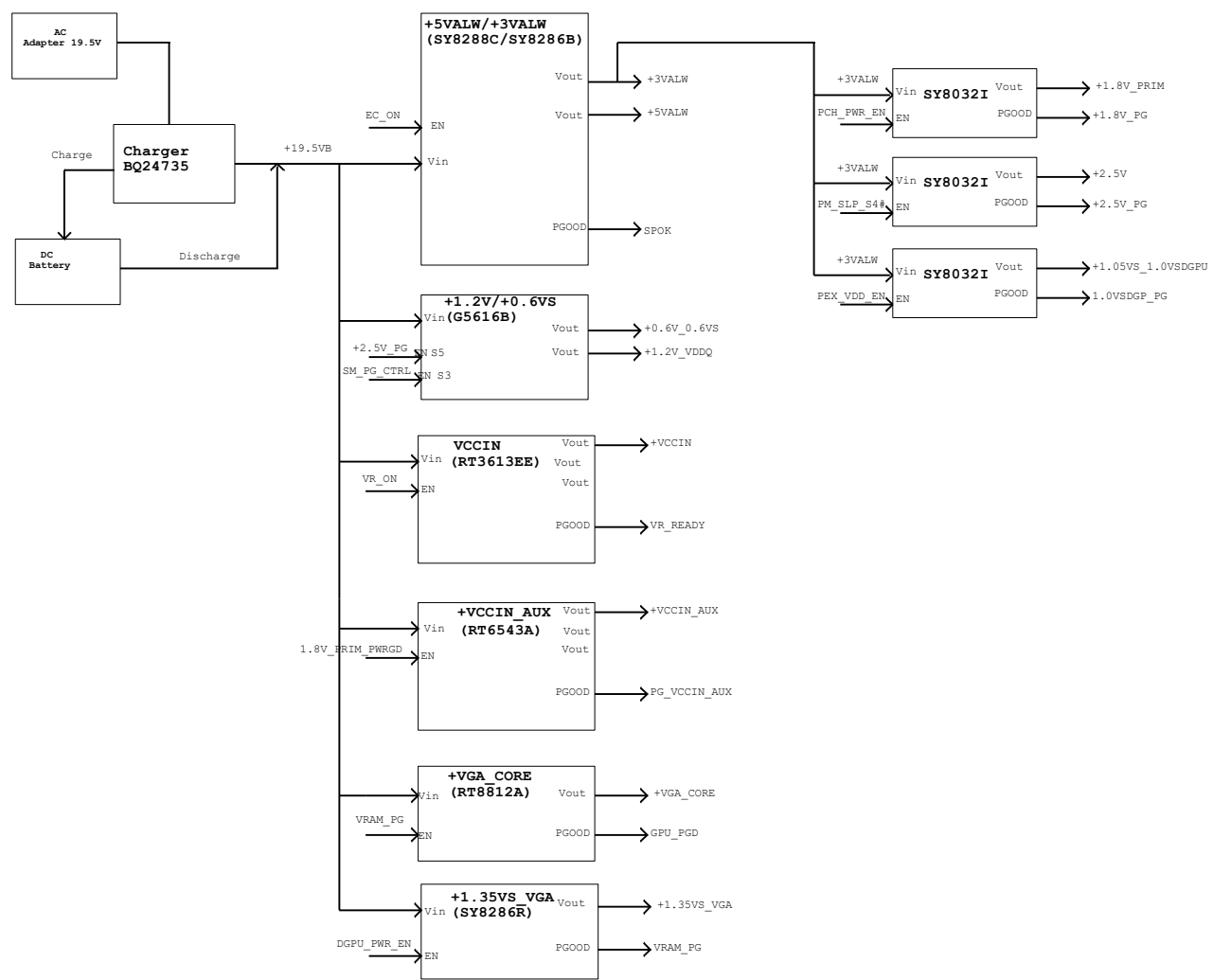


[DQA04-Power Map_ICL-U4+2_DDR4_Volume_S0ix]



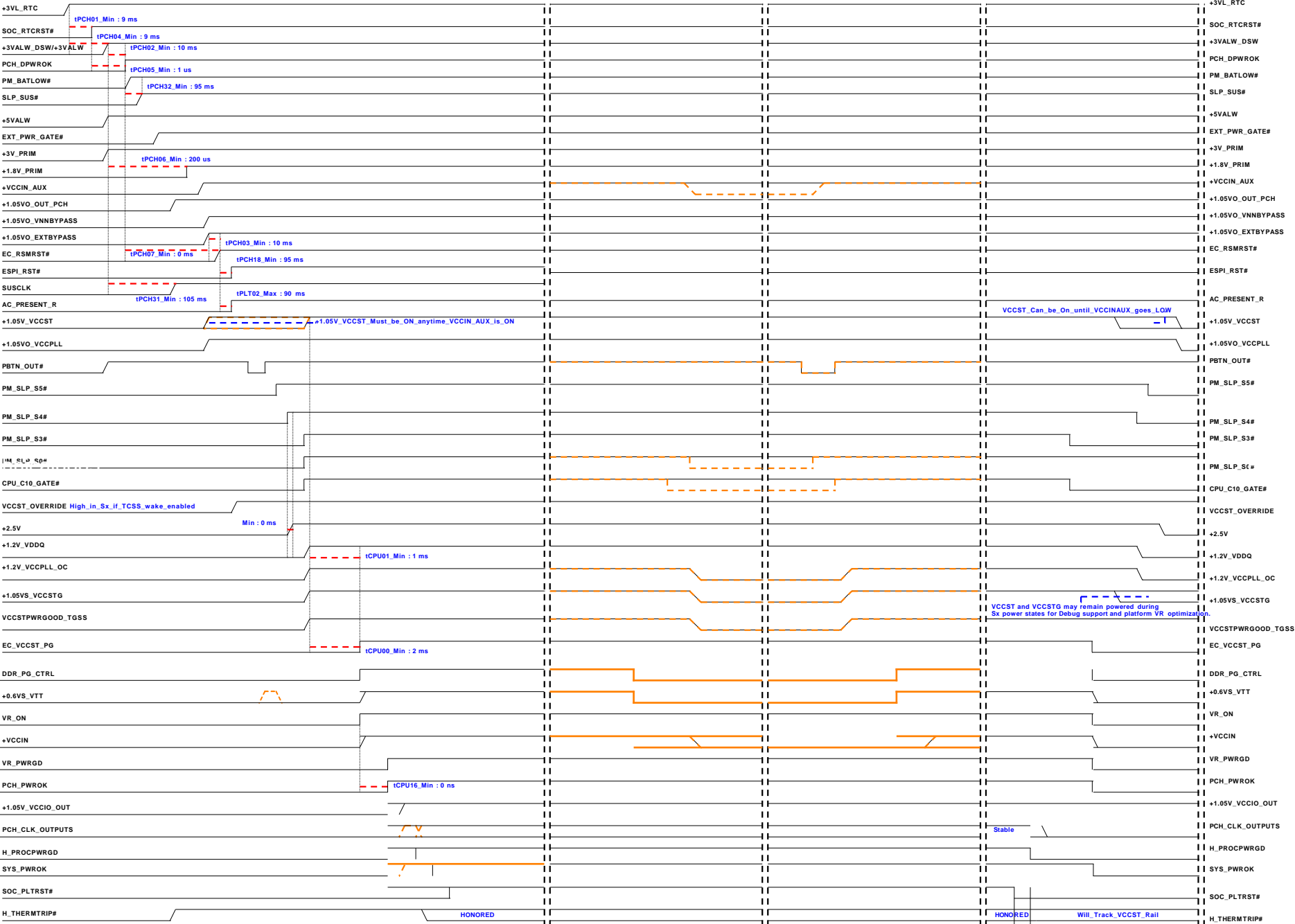


G3->S0

S0-> S0iX

S0iX ->S0

S0->S5



Board ID Table for AD channel

Vcc	3.3V				
Ra	100K +/-1%				
Board ID /PCB Revision	Rb	VbID min	VbID TYP	VbID Max	EC AD3
0 -> 0.1	0		0V	0.300V	0x00 - 0x0B
1 -> 0.2	12K +/-1%	0.347V	0.354V	0.36V	0x0C - 0x1C
2 -> 0.3	15K +/-1%	0.423V	0.430V	0.438V	0x1D - 0x26
3 -> 0.4	20K +/-1%	0.541V	0.550V	0.559V	0x27 - 0x30
4 -> 0.5	27K +/-1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5 -> 0.6	33K +/-1%	0.807V	0.819V	0.831V	0x3C - 0x46
6 -> 0.7	43K +/-1%	0.978V	0.992V	1.006V	0x47 - 0x54
7 -> 0.8	56K +/-1%	1.169V	1.185V	1.200V	0x55 - 0x64

BOM Structure Table

Funct i on	Stuf f	Un-Stuf f
UMA SKU	UMA@	DIS@ VGA@ EMIVGA@
dGPU SKU	DIS@ VGA@ EMIVGA@	UMA@
dGPU support GC6	GC6@	NGC6@
dGPU doesn't support GC6	NGC6@	GC6@
VRAM	1G@	
DMIC(SoC)	SOC_DMIC@	
DMIC(CODEC)	ALC_DMIC@	
CMC	CMC@	
TPM	TPM@	
HDD FFC CON (With Redriver)	HDD_RD@	HDD_FFC@
HDD FFC CON (Non Redriver)	HDD_FFC@	HDD_RD@
EMI Components	EMI@ BL_EMI@	@EMI@
ESD Components	ESD@ BL_ESD@	@ESD@
RF Components	RF@	@RF@
ME Connector	CONN@	
NC Components	@	
PRIM Design	PREM@	VOL@
Volume Design	VOL@	PREM@
EMMC	EMMC@	
CNVI	CNVI@	
WWAN	WWAN@	
SSD	SSD@	
Type C	TypeC@	
Type A	TypeA@	
Finger Print	FP@	
GLITCH	GLITCH@	
KB Backlight	KB_BKL@	
HDMI	HDMI20@	EDP2@
2 eDP	EDP2@	HDMI20@
SPI Touch	SOC_THP@	
For Signal Test	MP@	
JUMP (HW & PWR)	JUMP@	@JUMP@
JUMP (PWR)	VGAJUMP@	

HSIO Port Table

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	USB3.1 #1 / PCIe#1	USB3.0 Type C	NA	USB3.0 interface
1	USB3.1 #2 / PCIe#2	USB3.0 Type C	NA	USB3.0 interface
2	USB3.1 #3 / PCIe#3	USB3.0 Type A	NA	USB3.0 interface
3	USB3.1 #4 / PCIe#4	USB3.0 Type A	NA	USB3.0 interface
4	USB3.1 #5 / PCIe#5	dGPU	CLK0 & CLKREQ#0	PCIe interface
5	USB3.1 #6 / PCIe#6			
6	PCIe #7 / GbE / UFS2.0			
7	PCIe #8 / GbE / UFS2.0			
8	PCIe #9 / GbE	LAN	CLK1 & CLKREQ#1	PCIe interface
9	PCIe #10	WLAN+CNvio (NGFF_KeyE)	CLK2 & CLKREQ#2	PCIe interface
10	PCIe #11 / SATA0	HDD	NA	PCIe / SATA interface
11	PCIe #12 / SATA1a*	NA	NA	NA
12	PCIe #13 / GbE	SSD (NGFF Key M)	CLK4 & CLKREQ#4	PCIe / SATA
13	PCIe #14 / GbE			
14	PCIe #15 / SATA1b*			
15	PCIe #16 / SATA2			

Power State

STATE	SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)		HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
SOIX		LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

Load BOM Option Table

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	1G@/WWAN@/ALC_DMIC@/CNVI@/DEBUG@/DIS@/EMI@/BL_EMI@/EMMC@/ESD@/BL_ESD@/FP@/GC6@/GLITCH@/HDD_FFC@/HDMI20@/CMC@/MP@/SOC_DMIC@/SSD@/TPM@/TypeC@/VOL@/TypeA@/KB_BKL@/SOC_THP@
431ACX30L02(UMA)	WWAN@/ALC_DMIC@/CNVI@/DEBUG@/EMI@/BL_EMI@/EMMC@/ESD@/BL_ESD@/FP@/GLITCH@/HDD_FFC@/HDMI20@/CMC@/MP@/SOC_DMIC@/SSD@/TPM@/TypeC@/UMA@/VOL@/TypeA@/KB_BKL@/SOC_THP@

Load BOM Option Table for Baseline

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	1G@/ALC_DMIC@/DIS@/EMI@/ESD@/GC6@/GLITCH@/HDD_FFC@/HDMI20@/SOC_DMIC@/VOL@/VGA@/EMIVGA@
431ACX30L02(UMA)	ALC_DMIC@/EMI@/ESD@/GLITCH@/HDD_FFC@/HDMI20@/SOC_DMIC@/VOL@/UMA@

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59
SOC_SML0CLK SOC_SML0DATA	+3V_PRIM		TBC	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3V_PRIM		TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VL_EC	BAT	0x16	TBC	TBC
		CHGR	0x12	TBC	TBC
EC_SML1CLK EC_SML1DATA	+3VS	GPU	0x41	TBC	TBC
		THERMAL	0x48	0X91	0x90
		PCH	0x08h	TBC	TBC

I2C Address Table (TBC)

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C0	+3VS		0x0FH	TBC	TBC
			0x48H	TBC	TBC
I2C2	+3VS		TBC	TBC	TBC
I2C3	+3VS		0x2CH	TBC	TBC
ISH_I2C0	+1.8VS		0FH	TBC	TBC

Voltage Rails

Power Plane	Descript i on	S0	S0ix	S3	S4/S5
+20V_AD_P_IN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat t ery po wers upply	N/A	N/A	N/A	N/A
+19VB	AC or bat t ery po werr aill or po wercircut	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.0VS_DGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.0SV_VCCSTG	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	ON	OFF	OFF
+1.2V_VCCPLL_OD	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

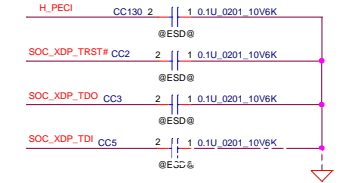
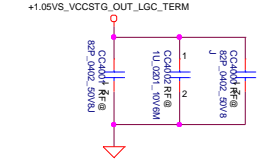
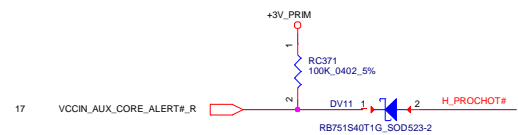
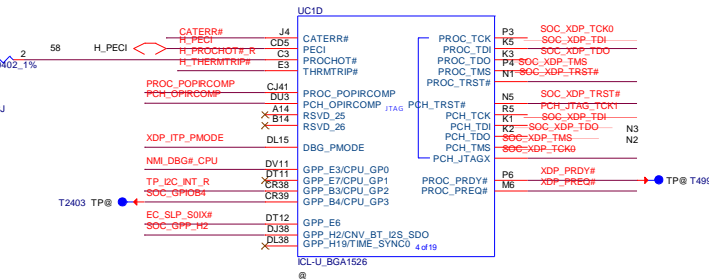
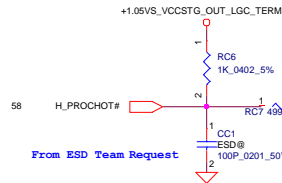
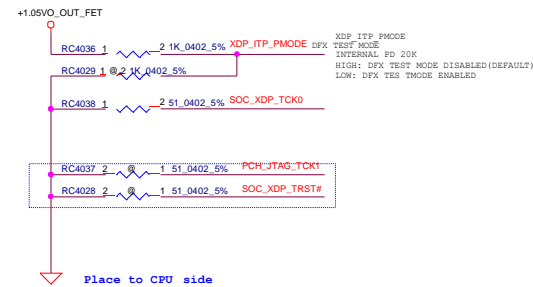
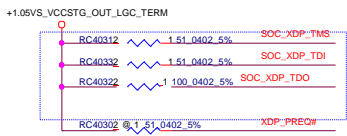
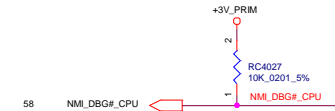
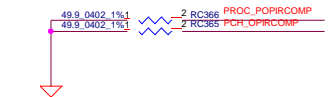
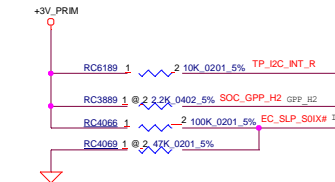
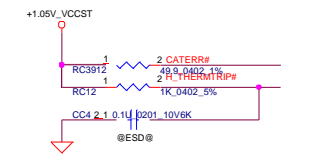
USB2.0 Port Table

USB2.0 Port	Device
1	USB Type-A (SB)
2	USB Type-A (SB)
3	USB Type-C (MB)
4	USB Card Reader (SB)
5	USB Camera
6	USB Finger print
7	USB Touch screen
8	NA
9	NA
10	NGFFBT





To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/9/25	Deciphered Date	2018/12/31	Title	ICL-U(1/14)DDI,MSIC,XDP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	LA-J951P
				Date	Wednesday, April 22, 2020
				Sheet	7 of 100

DDR4: Refer to 575034_ICL_U42_DDR4_T3_6L_Core_Schematics_Rev0p7

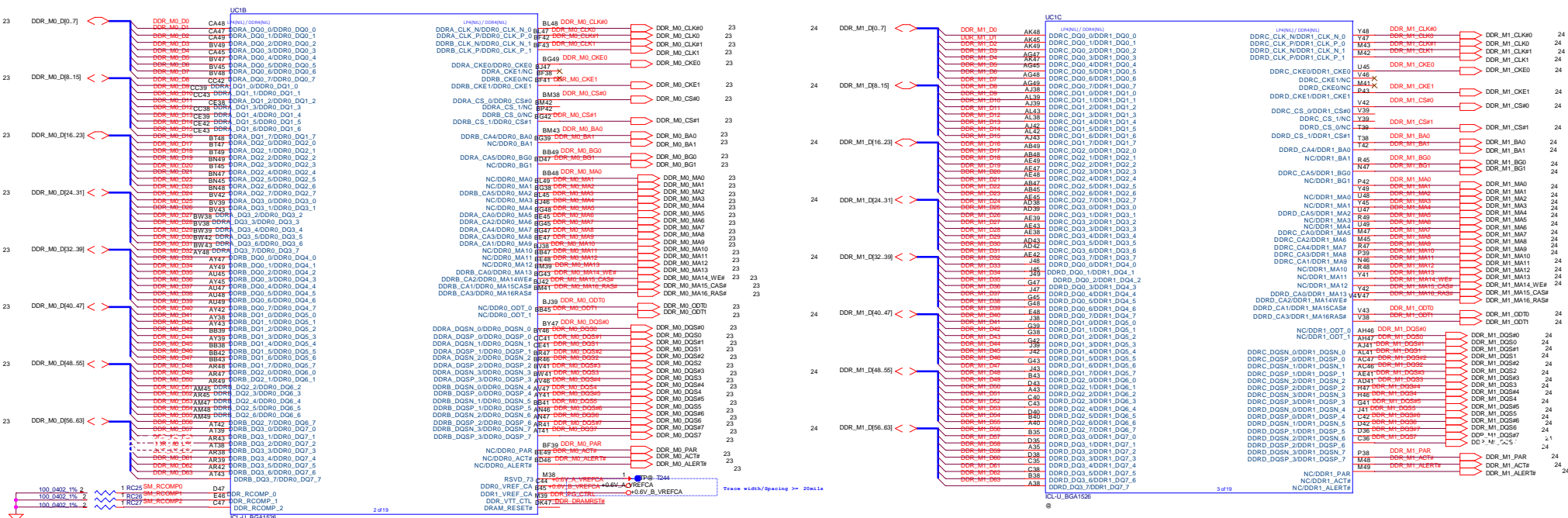
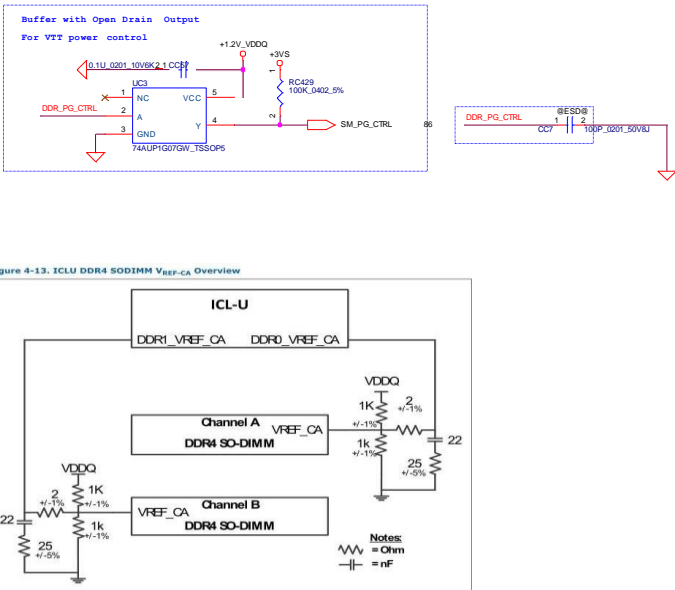
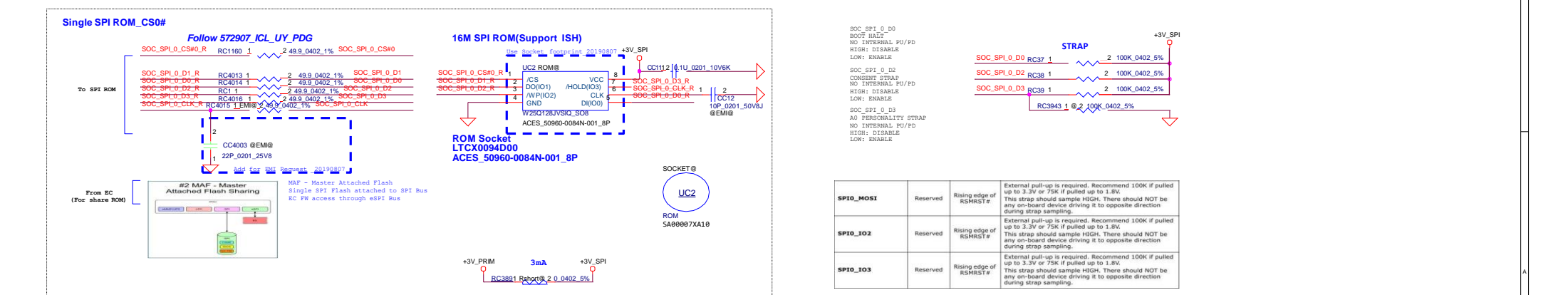
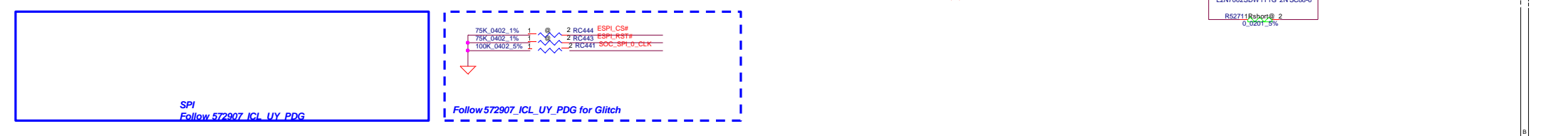
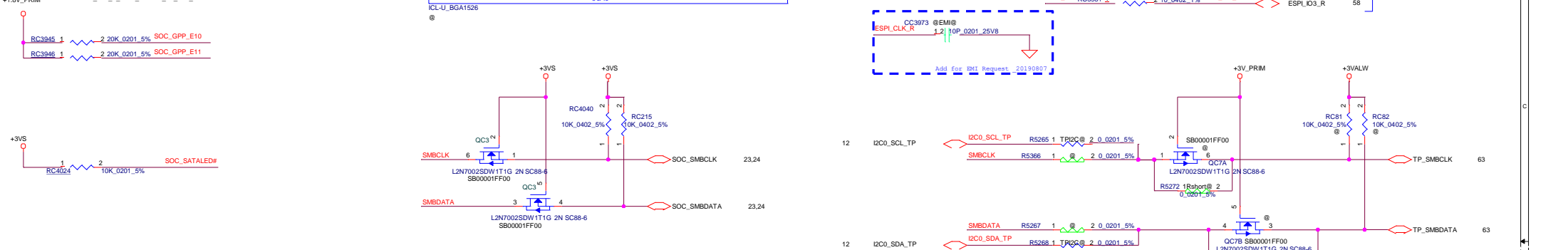
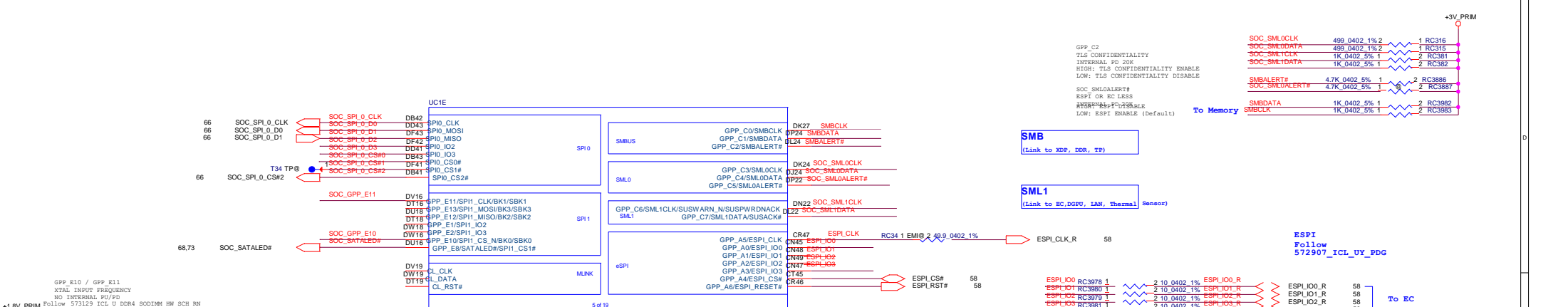


Figure 4-13. ICLU DDR4 SODIMM VREF-CA Overview



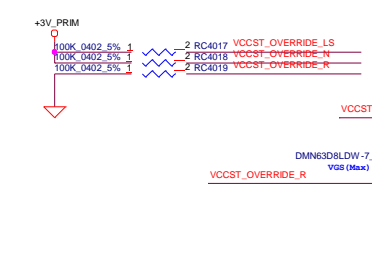
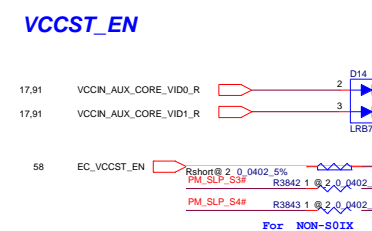
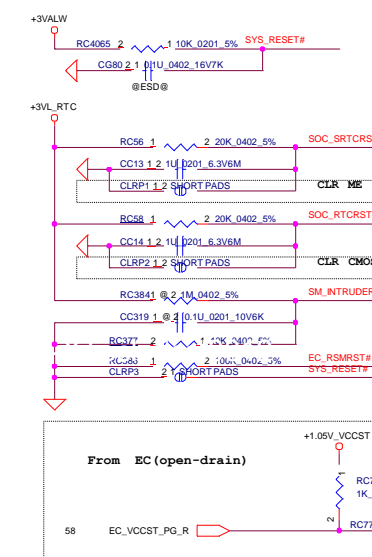


SPI0_MOSI		Reserved	Rising edge of RS#MOSI#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2		Reserved	Rising edge of RS#MOSI#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3		Reserved	Rising edge of RS#MOSI#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

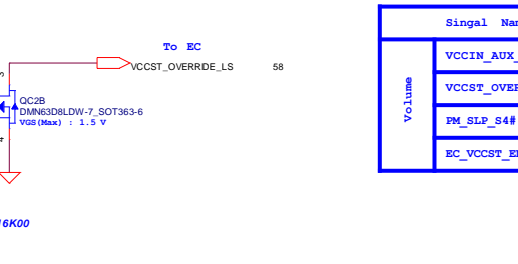
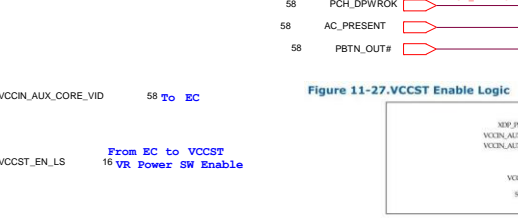
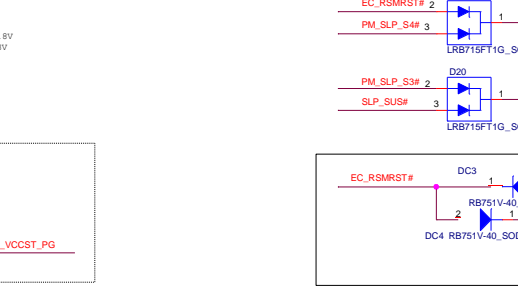
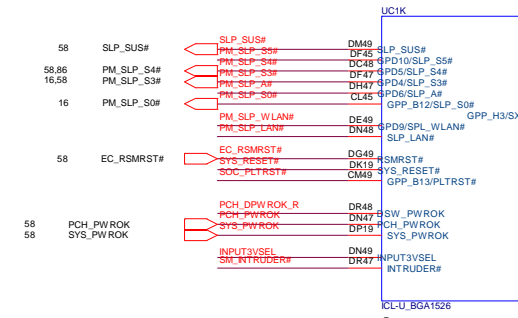
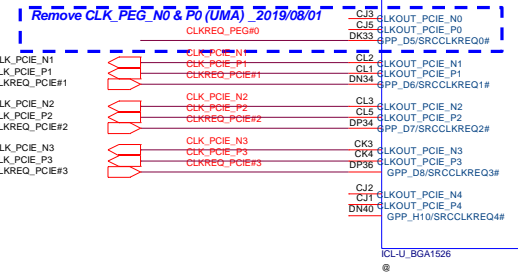
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/05/07	Deciphered Date	2019/12/31	Title
				ICL-U(3/12)SPI,ESPI,SMB,LPC
				LA-J951P
				Date: Wednesday, April 22, 2020 Sheet 9 of 100

Change RC3990 to un-pop for no use (UMA) 2019/08/01

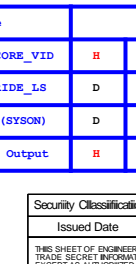
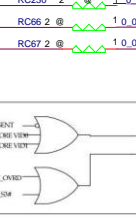
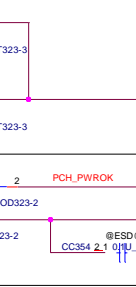
Follow 573129_ICL_U_DDR4_SODIMM_HW_SCH_RN & 572907_ICL_UY_PDG for Glitch



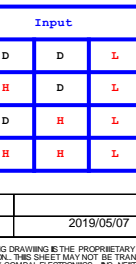
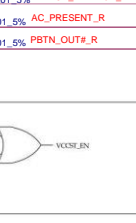
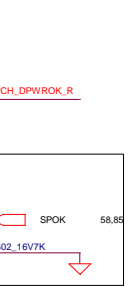
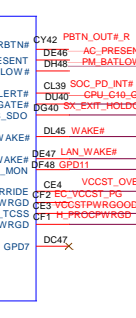
LAN
WLAN
SSD



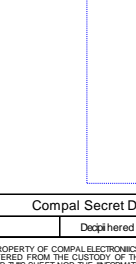
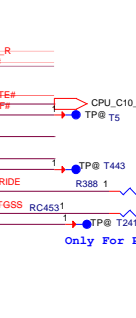
RTC
Xtal



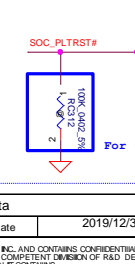
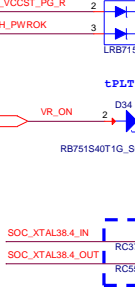
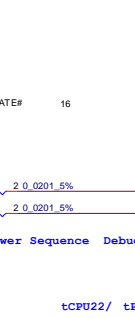
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_H1V/SRCLKREQ#



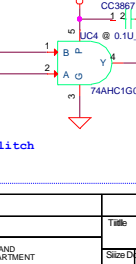
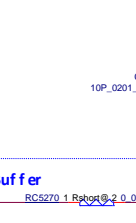
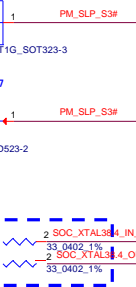
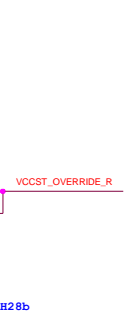
SOC_RTCX1
SOC_RTCX2
SOC_RTCRST#
SOC_RTCRST#
SUSCLK_R
SOC_XTAL38.4_IN
SOC_XTAL38.4_OUT
XCLK_BIASREF



INPUT3VSEL
3V SELECT STRAP
HIGH: 3.0V +/-5%
LOW: 3.3V +/-5%
Follow 573129_ICL_U_DDR4_SODIMM_HW_SCH_RN



PM_BATLOW#
WAKE#
LAN_WAKER#
INPUT3VSEL
SOC_PD_INT#
SUSCLK_R
CPU_C10_GATE#
AC_PRESENT_R



Follow 573129_ICL_U_DDR4_SODIMM_HW_SCH_RN

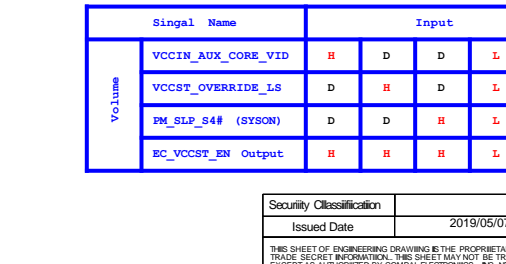
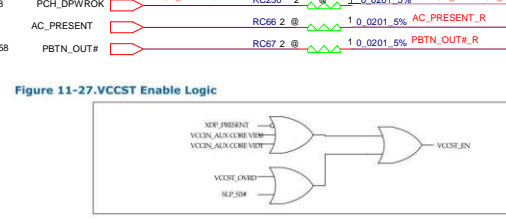
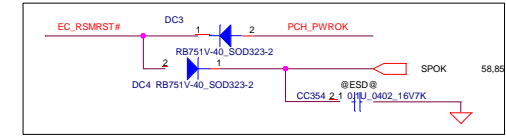
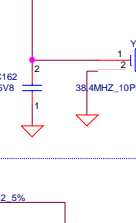
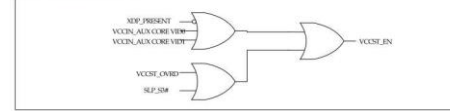
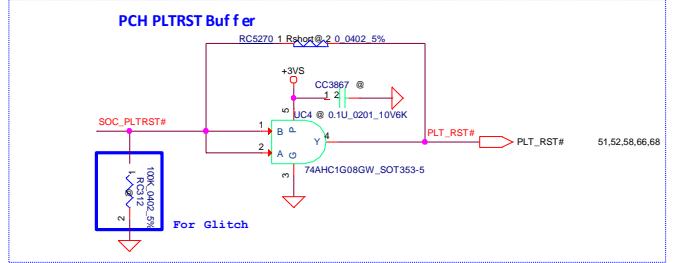
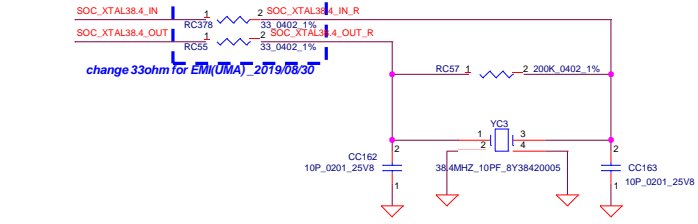
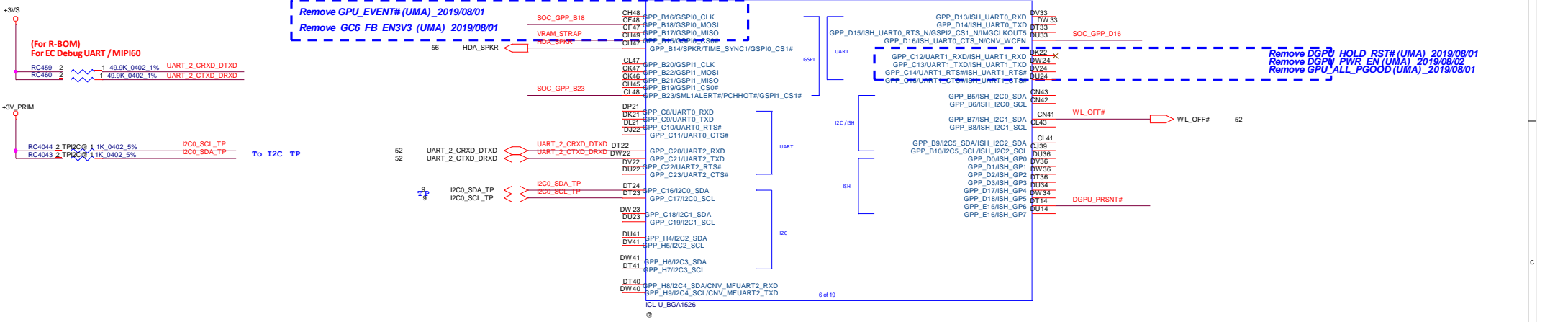


Figure 11-27.VCCST Enable Logic



Sigal Name	Input
VCCIN_AUX_CORE_VID	H D D L
VCCST_OVERRIDE_LS	D H D L
PM_SLP_S4# (SYSN)	D D H L
EC_VCCST_EN Output	H H H L



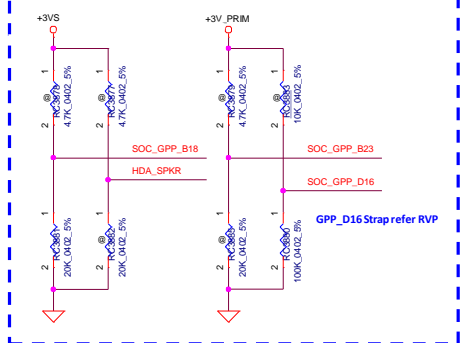


Remove DGPU_PWR_EN PU to +3VS (UMA) _2019/08/02

Remove GPU_EVENT# (UMA) _2019/08/01
Remove GC6_FB_EN3V3 (UMA) _2019/08/01

Remove DGPU_HOLD_RST# (UMA) _2019/08/01
Remove DGPU_PWR_EN (UMA) _2019/08/02
Remove GPU_ALL_PGOOD (UMA) _2019/08/01

Strap Pin



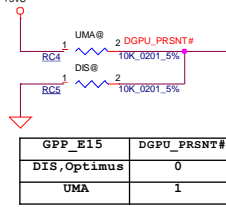
GPP_B23
CPUSSC CLOCK FREQ
INTERNAL PD 20K
HIGH: 19.2 Mhz (form internal divider)
LOW: 38.4 Mhz (direct form crystal) (Default)

GPP_B18
No Reboot
INTERNAL PD 20K
HIGH: No Reboot
LOW: Reboot Enable (Default)

SPFR
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: Top swap enable
LOW: Disable (Default)

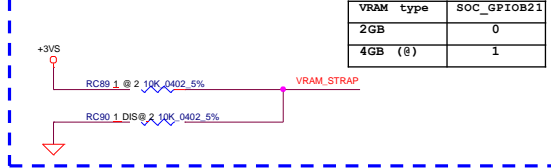
GPP_D16
MFX MODE DET STRAP
Follow 573129_ICL_U_D0R4_S0D1M0_HW_SCH_RN_1P0

For BIOS Verify UMA/DIS SKU

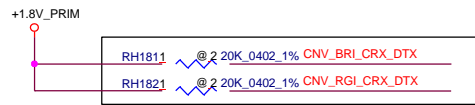
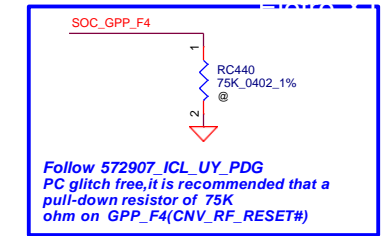
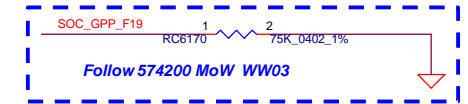
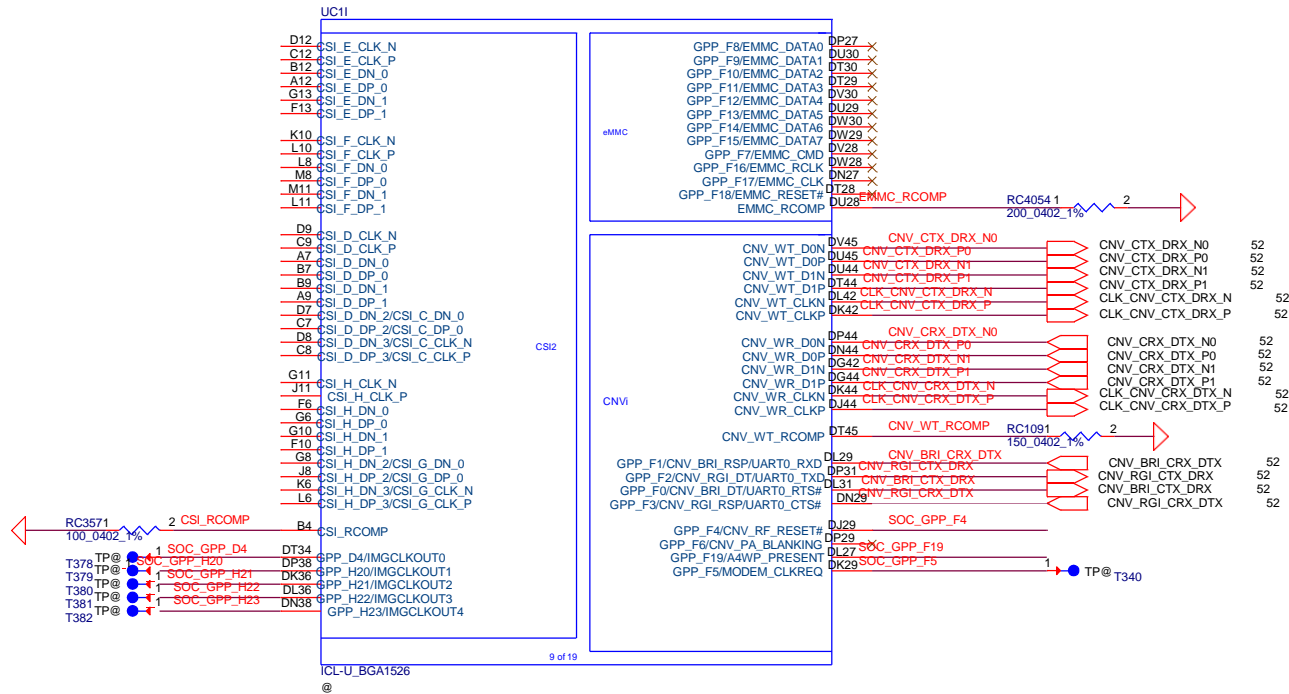


GPP_E15	DGPU_PRSENT#
DIS,Optimus	0
UMA	1

VRAM Strap Pin



VRAM type	SOC_GPIOB21
2GB	0
4GB (E)	1



CNV_RGI_CTX_DRX

M.2 CNVi MODES

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.

NO INTERNAL PU/PD

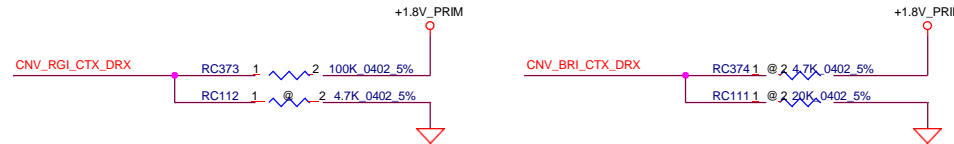
CNV_BRI_CTX_DRX

XTAL SEL

0 = 38.4/19.2MHZ (DEFAULT)

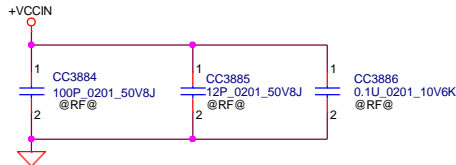
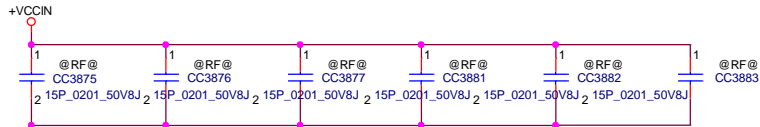
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K

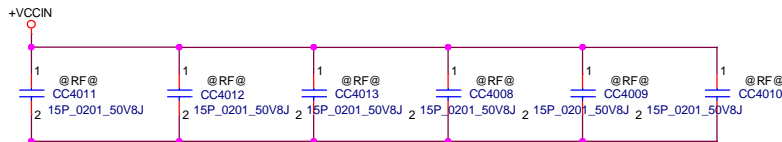


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/05/07	Deciphered Date	2019/12/31	Title	ICL-U(8/13)CSL,CNV
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	LA-J951P
				Date:	Wednesday April 22, 2020
				Sheet	14 of 100
				Rev	0.1

FIVR Decoupling Caps -PLACE < 5mm from SOC VCCIN

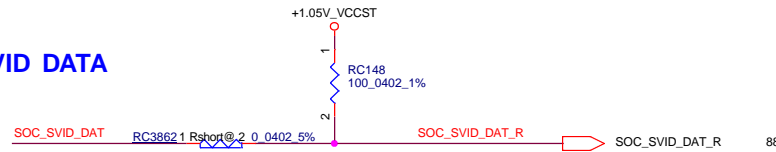


Add for RF Request _20190807

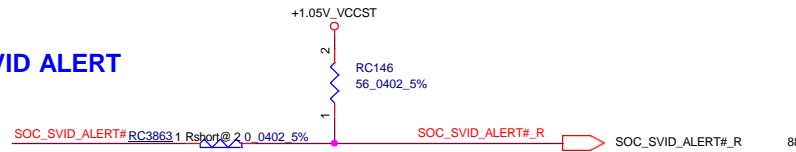


Add for RF Request _20190807_pwr

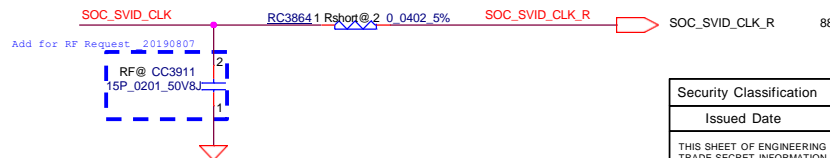
SVID DATA



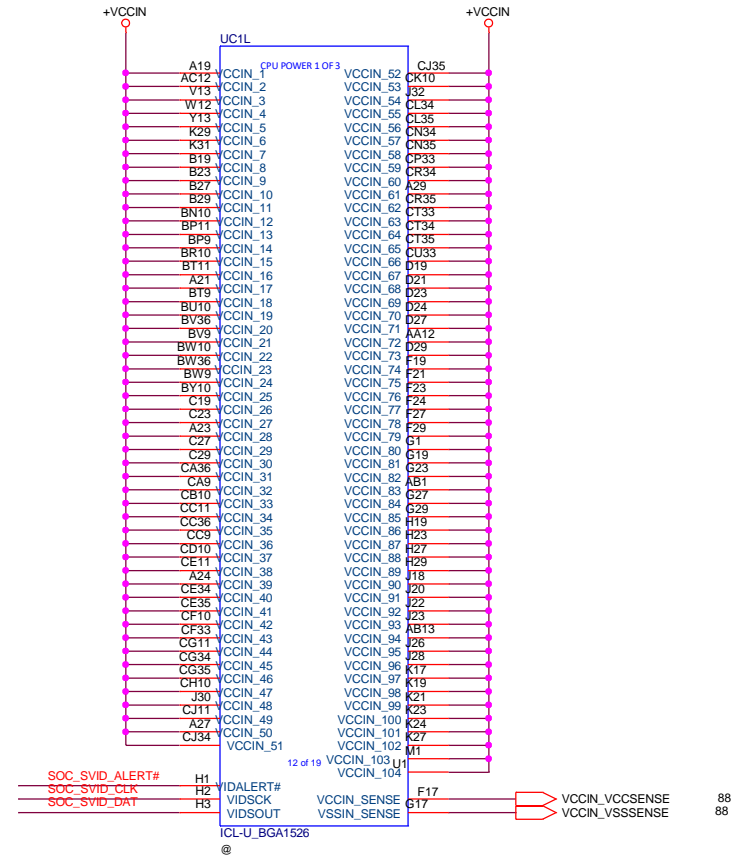
SVID ALERT



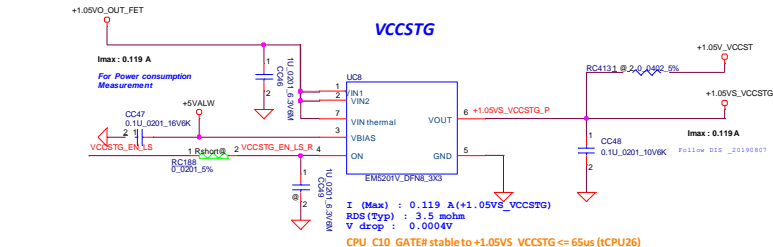
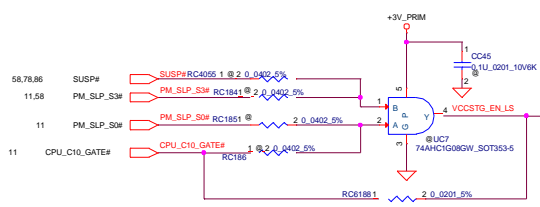
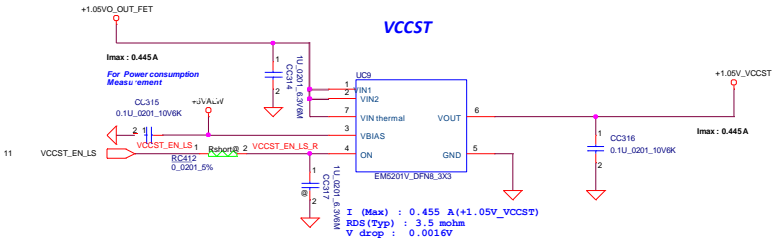
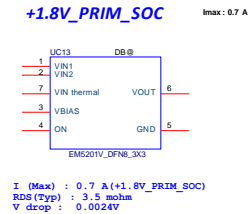
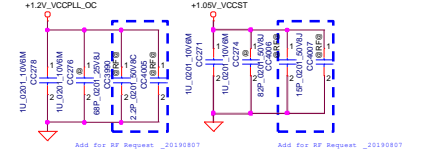
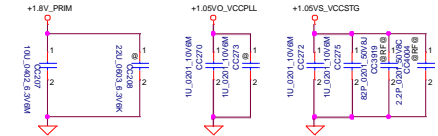
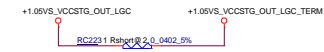
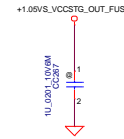
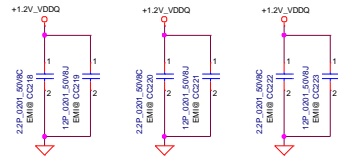
SVID CLOCK



Add for RF Request _20190807

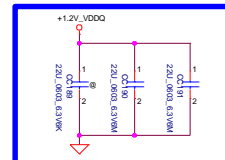


Security Classification		Compal Secret Data		Title	
Issued Date	2019/05/07	Deciphered Date	2019/12/31	ICL-U(9/13)Power, SVID	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	Rev
				LA-J951P	0.1
Date: Wednesday April 22, 2020		Sheet 15 of 100			

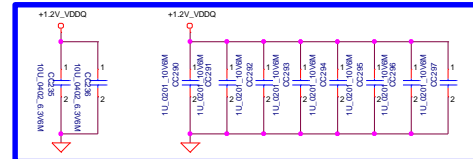


Volume	Premium
VccSTG and VccST are merged and gated by SLP_S4#	VccSTG gated by CPU_C10_GATE#
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by CPU_C10_GATE #
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1_05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches

Place on CPU Side
22uF* 2 + 22uF* 1 (Reserved)



Place on opposite of CPU Side
1uF* 8
10uF* 2



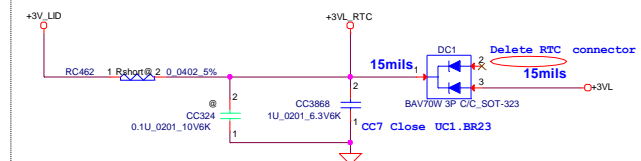
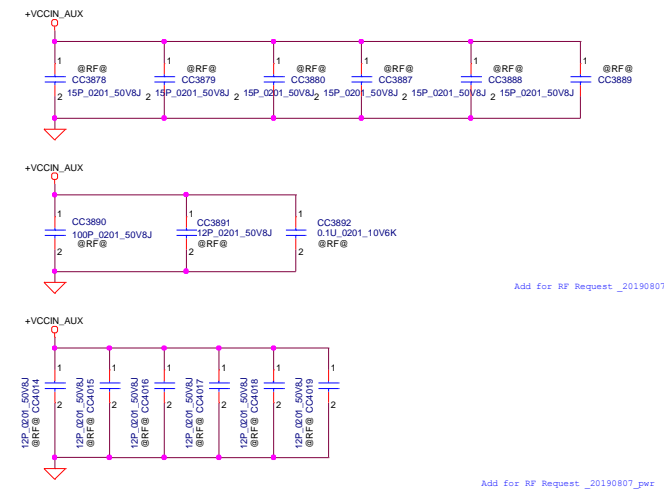
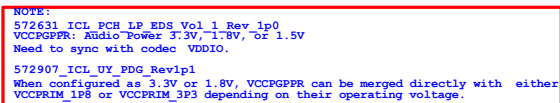
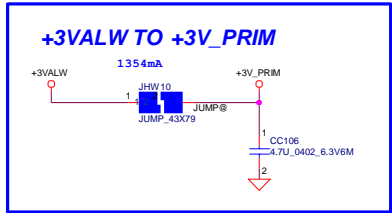
For NON-SOIX

+1.2V_VDDQ +1.2V_VCCPLL_OC

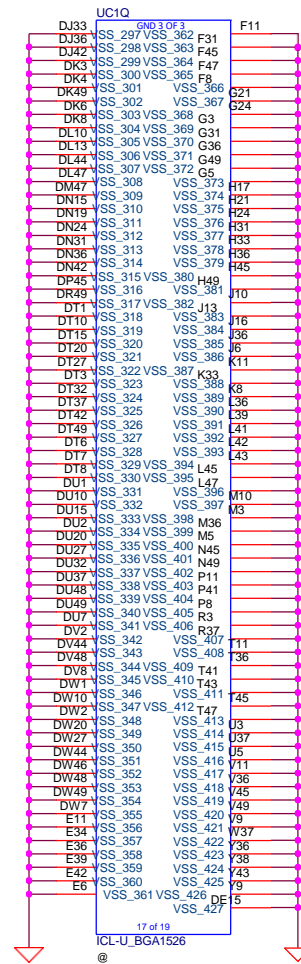
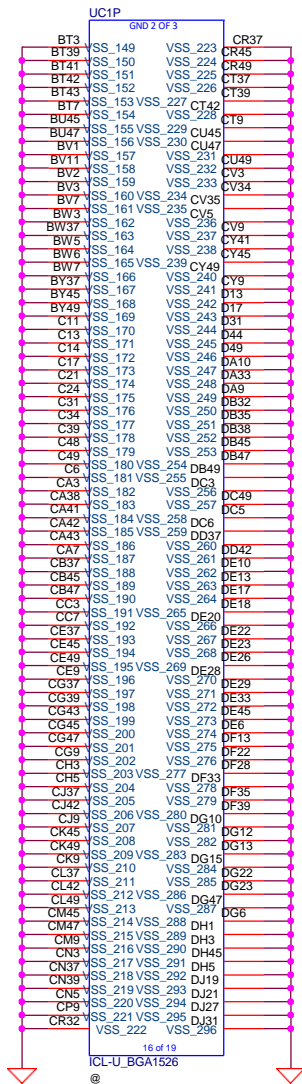
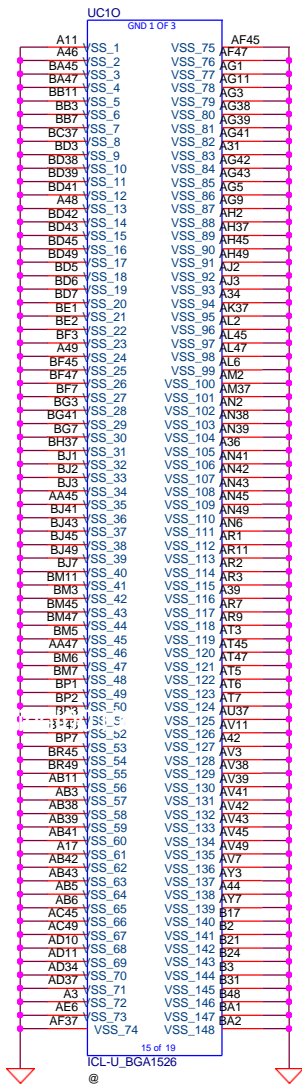
RC2541 @ 2.0_0402_5%

I_{max}: 0.152A

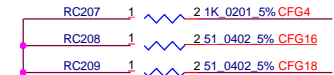
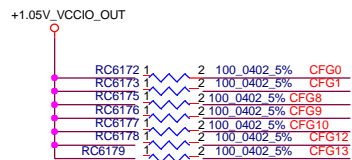
I (Max) : 0.152 A(+1.2V_VCCPLL_OC)
RDS(Typ) : 3.5 mohm
V drop : 0.0005V



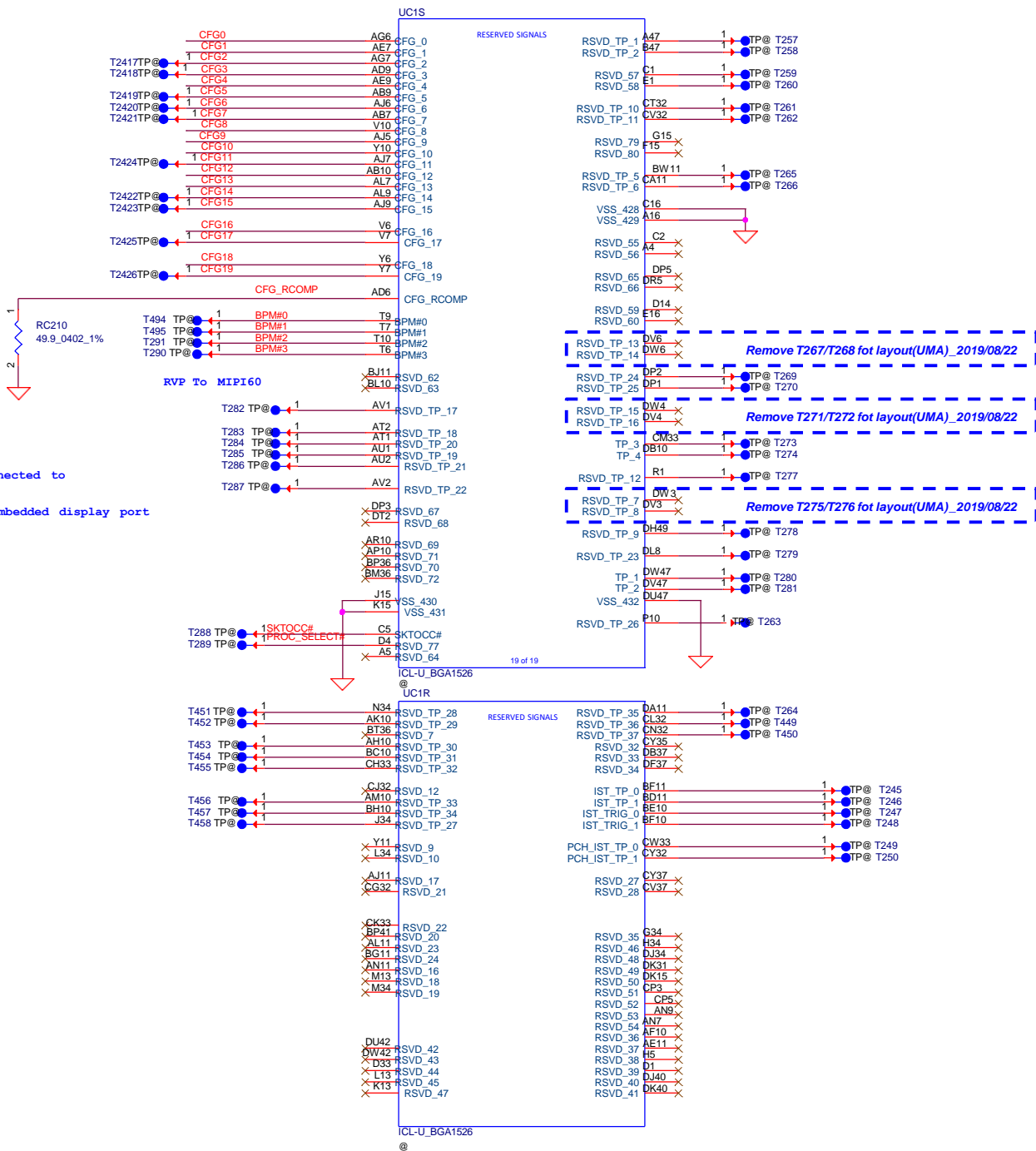
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> ICL-U(11/13)Power	
Issued Date	2019/05/07	Deciphered Date	2019/12/31	Title LA-J951P	Size/Document Number LA-J951P
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date: Wednesday, April 22, 2020	Rev 0.1
				Sheet 17 of	100



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2019/05/07		Title	
		Deciphered Date		ICL-U(12/13)GND	
		2019/12/31		Size/Document Number	
				LA-J951P	
				Date: Wednesday April 22, 2020	
				Sheet 18 of 100	
				Rev 0.1	



CFG4
Display port presence strap
0 : Enable
An external display port device is connected to the embedded displayport
1 : Disable
No physical display port attached to embedded display port



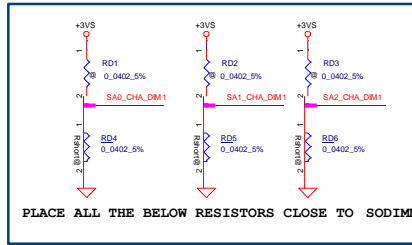
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2019/05/07		Title	
		Deciphered Date		2019/12/31	
				ICL-U(13/13)RSVD.CFG	
				Size/Document Number	
				LA-J951P	
				Date: Wednesday, April 22, 2020	
				Sheet 19 of 100	
				Rev 0.1	

CHANNEL-M0

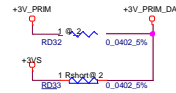
REVERSE TYPE

Non-Interleaved Memory

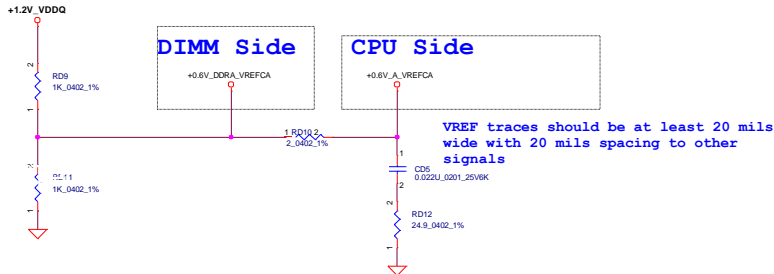
TOP: JDIMM1 CONN Non-ECC DIMM



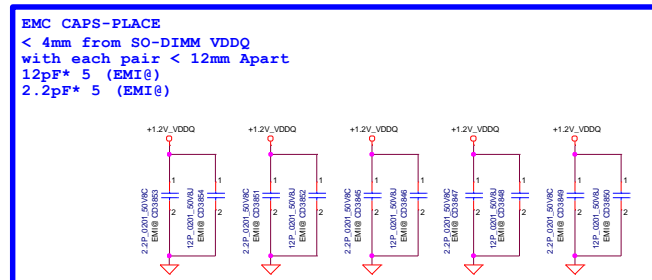
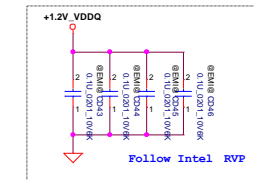
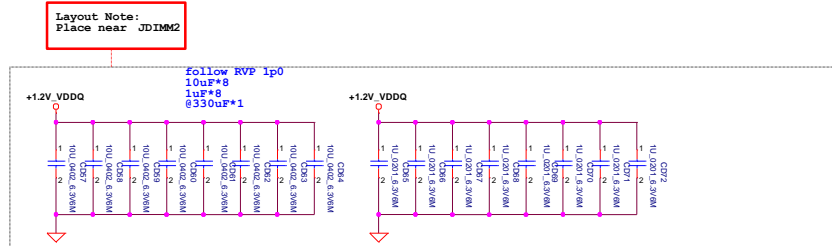
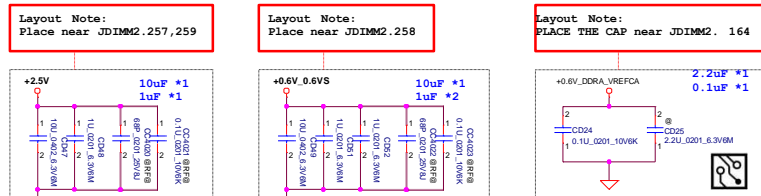
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



PLACE NEAR TO PIN



Decoupling Cap_Channel A

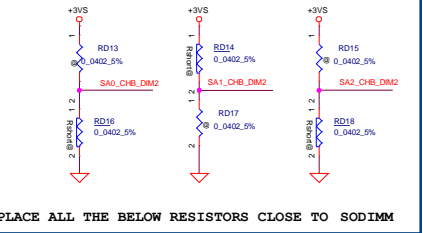


CHANNEL-M1

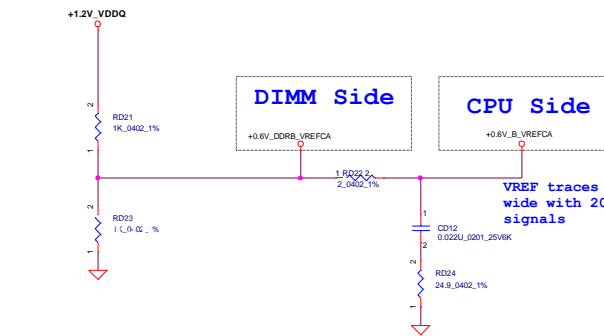
STD (5.2 mm)

Non-Interleaved Memory

TOP: JDIMM2 CONN Non-ECC DIMM

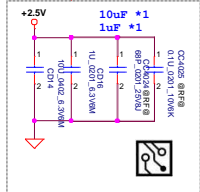


SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

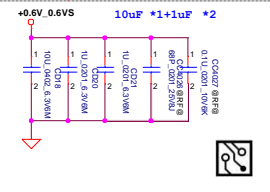


Decoupling Cap_Channel B

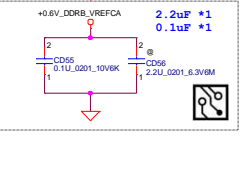
Layout Note:
Place near JDIMM1.257,259



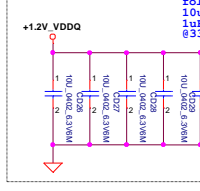
Layout Note:
Place near JDIMM1.258



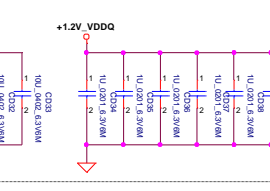
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM1



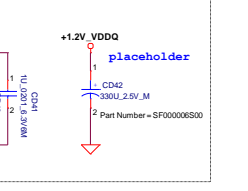
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1



Update Table 4-26 for DDR4 SODIMM Decoupling Caps
572907_ICL_UY_FDG_Rev0p7

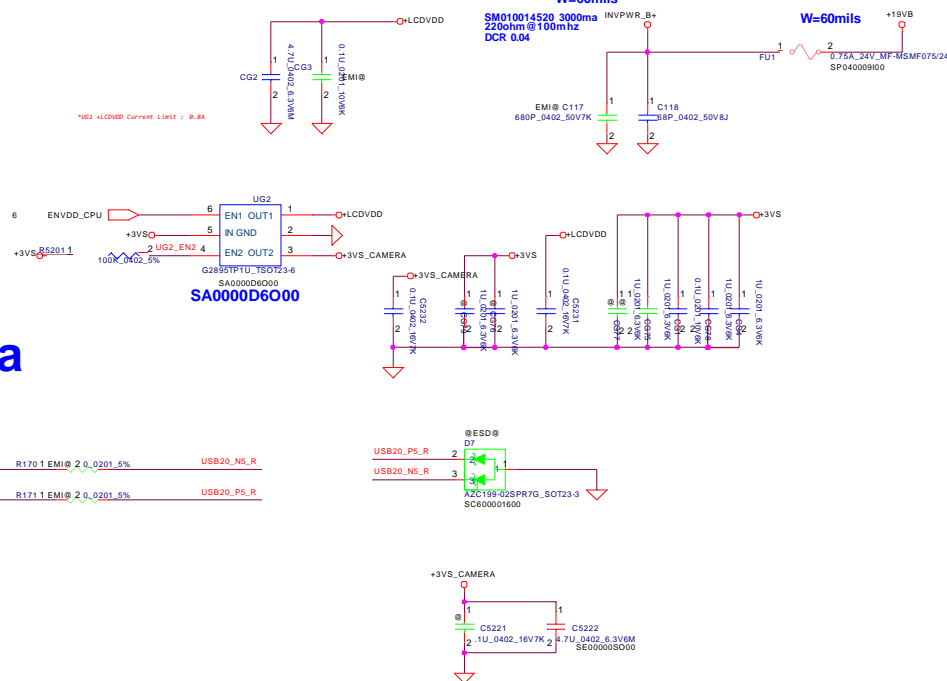
Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10uF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1uF (0402)
		placeholder	1x 330uF (7343)
		Place on VTT plane close to DIMM	2x 10uF (0603)
	VTT	1 cap stuffed, 1 placeholder	
		Place on VTT plane close to DIMM	4x 1uF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10uF (0603)
		DIMM pin side, 1 per DIMM	2x 1uF (0402)
	VDDSPD	Place close to DIMM	2x 0.1uF (0402)
		Place close to DIMM	2x 2.2uF (0402)

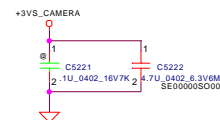
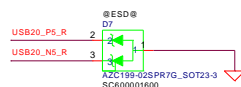
Note:
1. Total quantity is referring to 2 channels.

Security Classification		Compall Secret Data		Compall Secret Data	
Issued Date	2019/05/07	Deciphered Date	2019/12/31	Compall Secret Data	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Rev 0.1	
DDR4 CHM1: DIMM1				Rev 0.1	
LA-1951P				Rev 0.1	
Date: Wednesday, April 22, 2020				Rev 0.1	

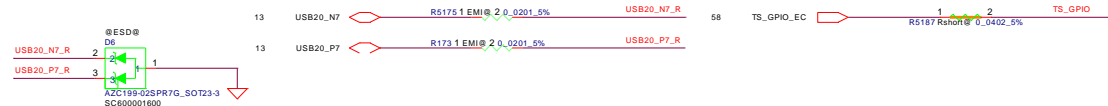
eDP Power



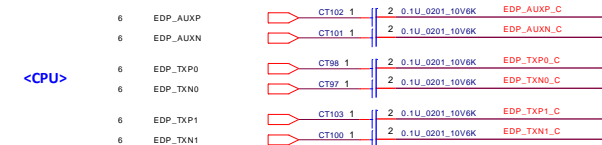
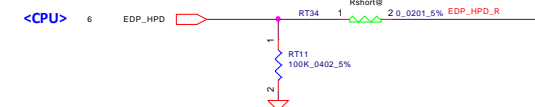
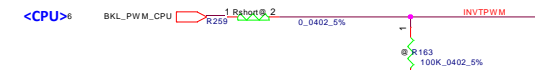
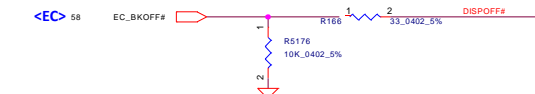
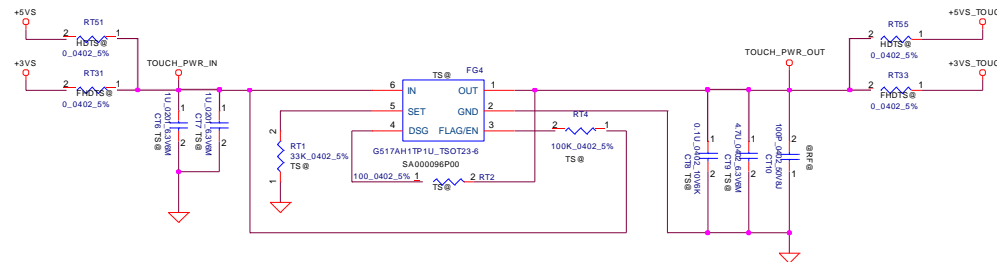
Camera



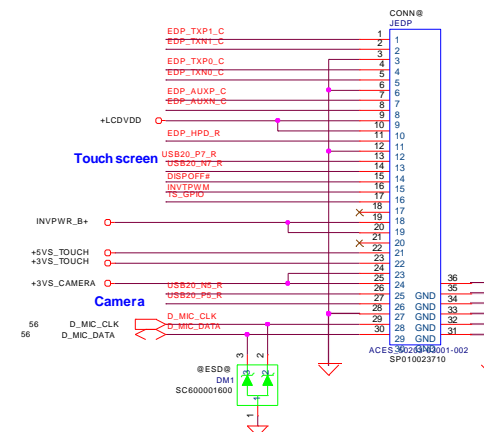
Touch Screen



Touch Screen Power Selection:TS@/HDTs@



eDP



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2019/10/08	Declassified Date	2021/10/08	Title	eDP CONN/Camera/TS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	Rev	
				LA-J952P		0.2
				Date: Wednesday, April 22, 2020	Sheet 8 of 100	

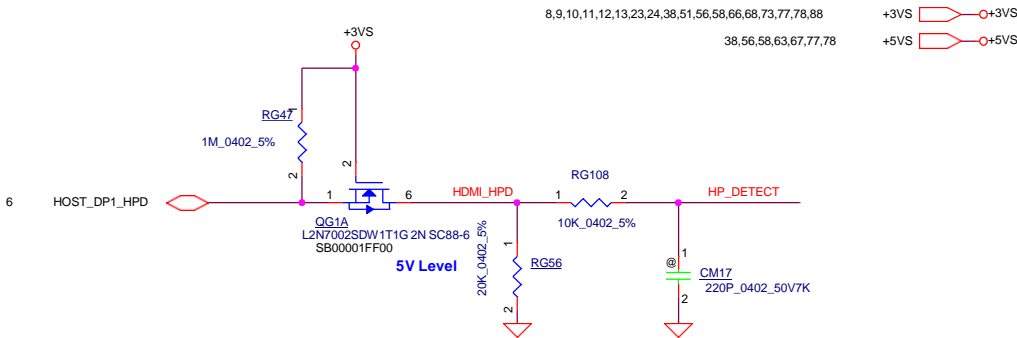
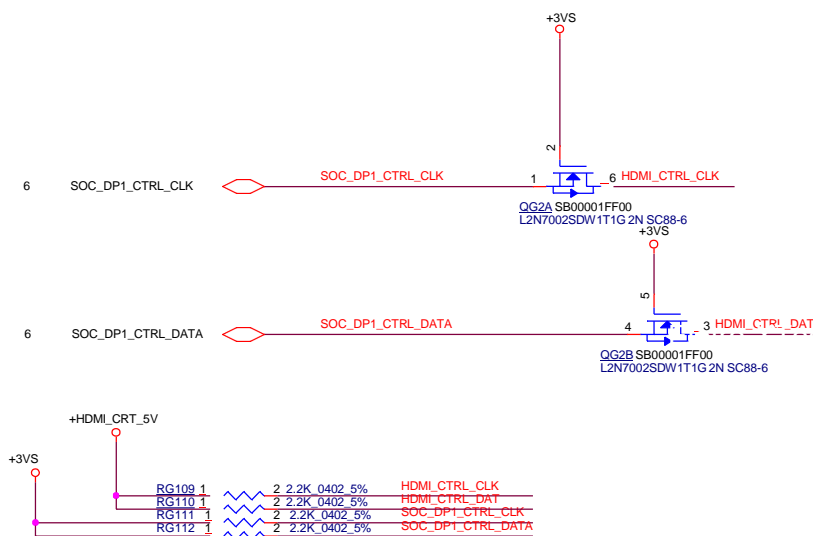
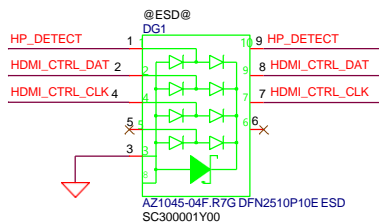
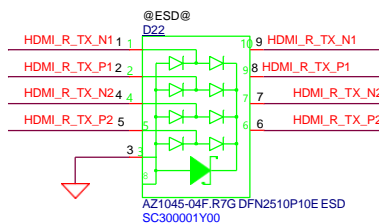
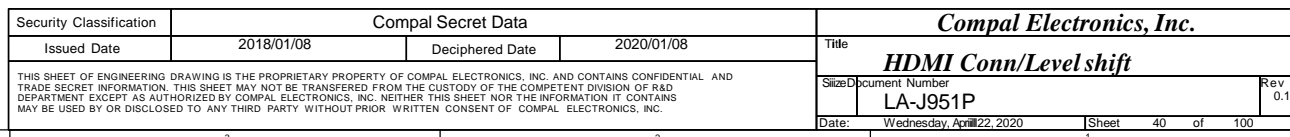
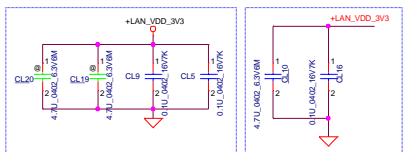
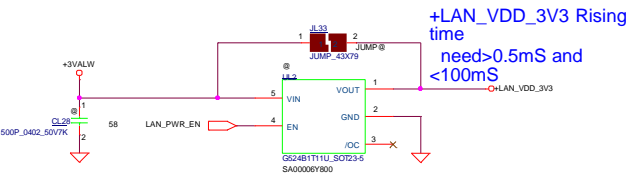


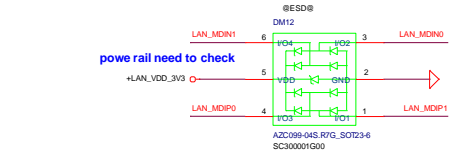
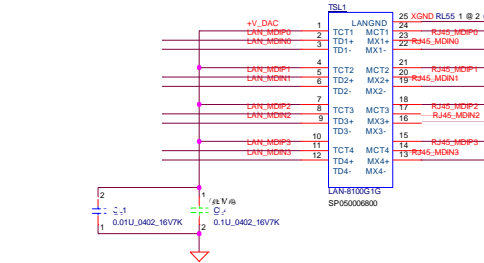
Table 1-4. Digital Display Interface Signal Mapping

The diagram displays eight signal traces over a common time axis. The top trace, SI phase:R5_20ohm_RP_150ohm, shows a periodic signal with a period of 2.0 ns and a 1% duty cycle. Below it, the HDMI signals are shown as transitions between high and low states. The HDMI signals are: HDMI_CLKP, HDMI_CLKN, HDMI_TX_N2, HDMI_TX_P2, HDMI_TX_P1, HDMI_TX_N1, HDMI_TX_P0, and HDMI_TX_N0. Each signal trace is labeled with its name and a value of 1. The signal transitions are marked with a '1' and a '2' at the top of the transition, indicating the signal level before and after the transition. The signal transitions are labeled with the signal name and a value of 1. The signal transitions are labeled with the signal name and a value of 1.

[illegible]

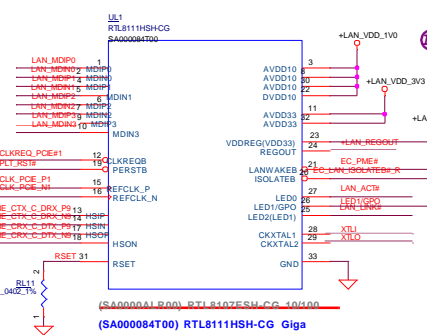


CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32



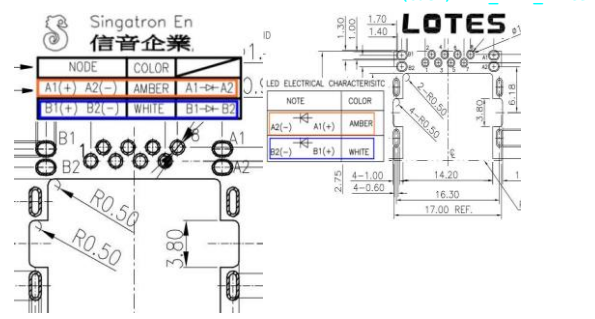
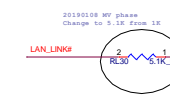
+LAN_VDD_3V3 Rising time
need>0.5mS and
<100mS

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay



CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 - CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



8,9,10,11,12,13,23,24,38,40,51,56,58,66,68,73,77,78,88
9,11,17,51,56,63,66,78,85,86,87,91
9,14,16,17,58,78,87

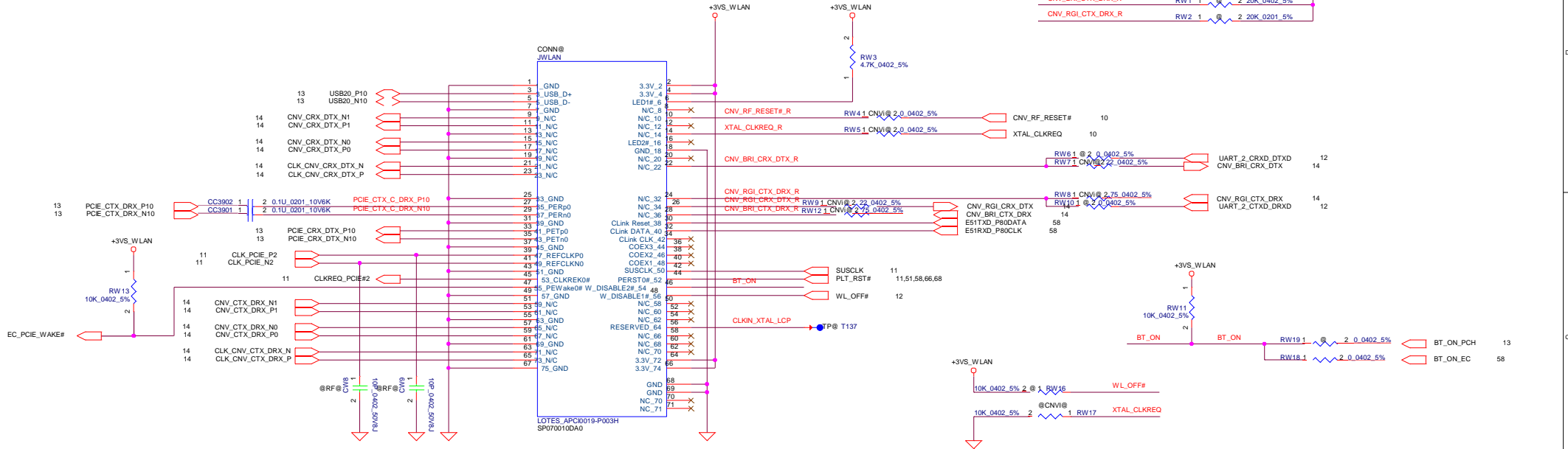
+3VS
+3VALW
+1.8V_PRIM

2018/06/22

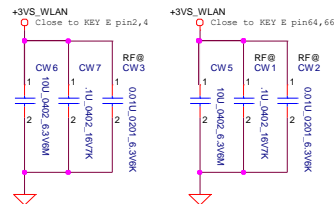
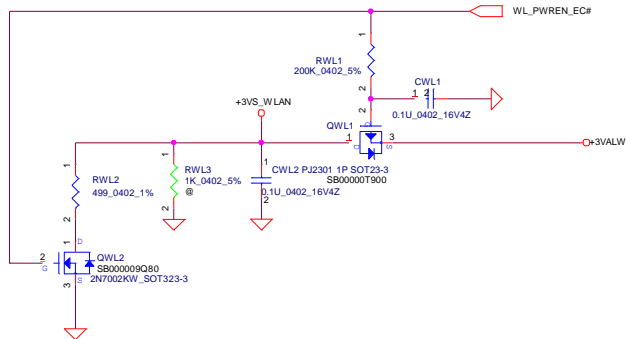
ADD RC183

ADD RC72 and Change from 49.9K to 20K

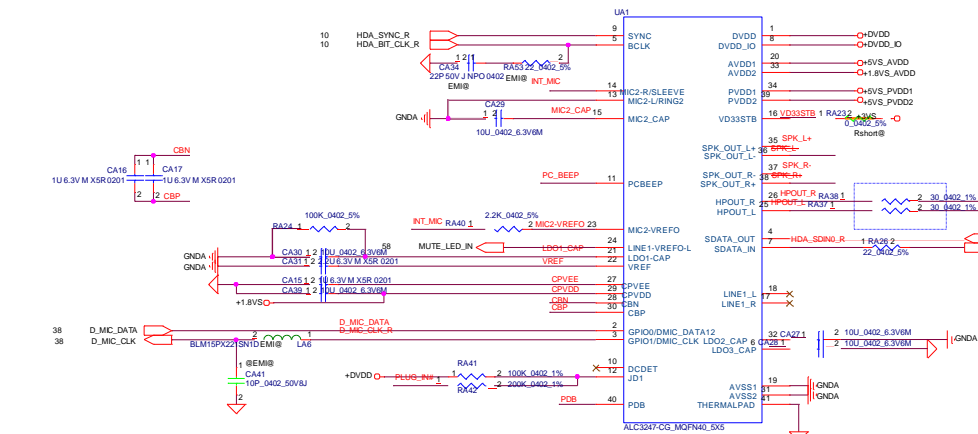
CNV_BRI_CTX_DRX_R RW1 1 2 20K 0402 5%
CNV_RGL_CTX_DRX_R RW2 1 2 20K 0201 5%



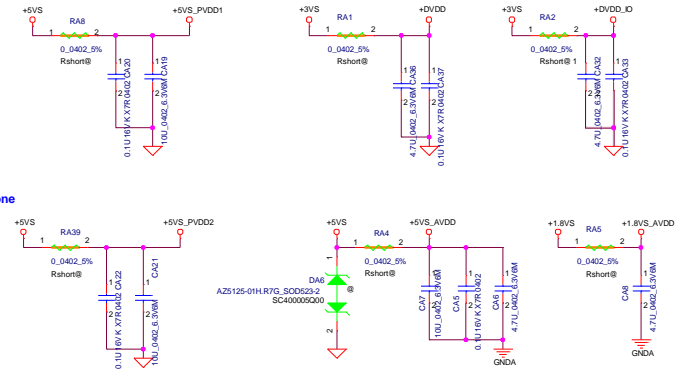
Active Low



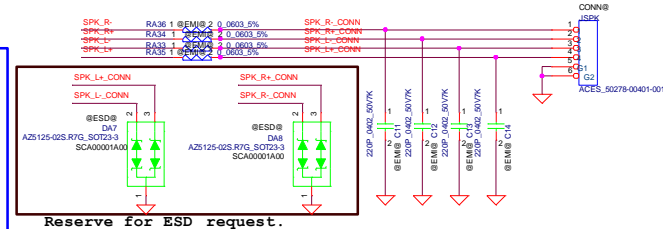
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2019/10/08	Deciphered Date	2021/10/08	Title WLAN-BT	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Document Number LA-J952P	Rev 0.1
				Date: Wednesday, April 22, 2020	Sheet 52 of 100



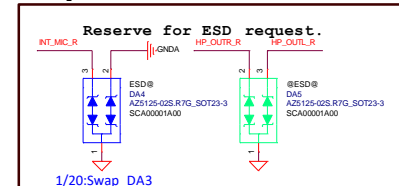
Headphone



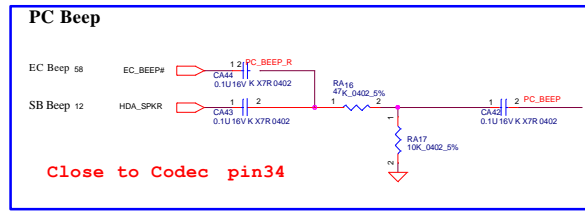
Internal SPK wide 40 MIL



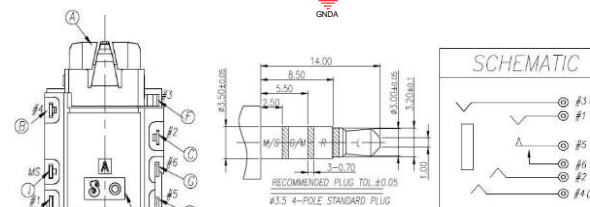
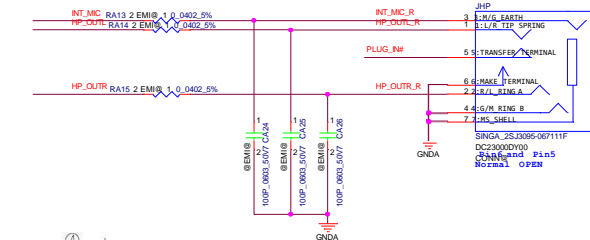
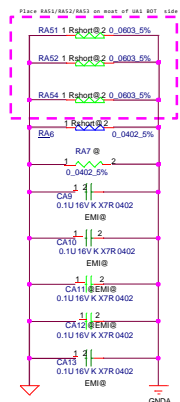
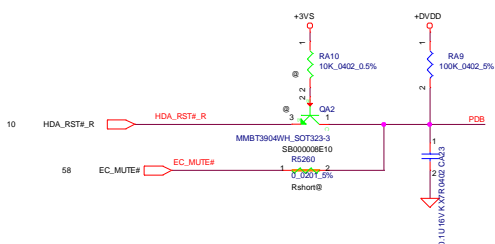
Reserve for ESD request.

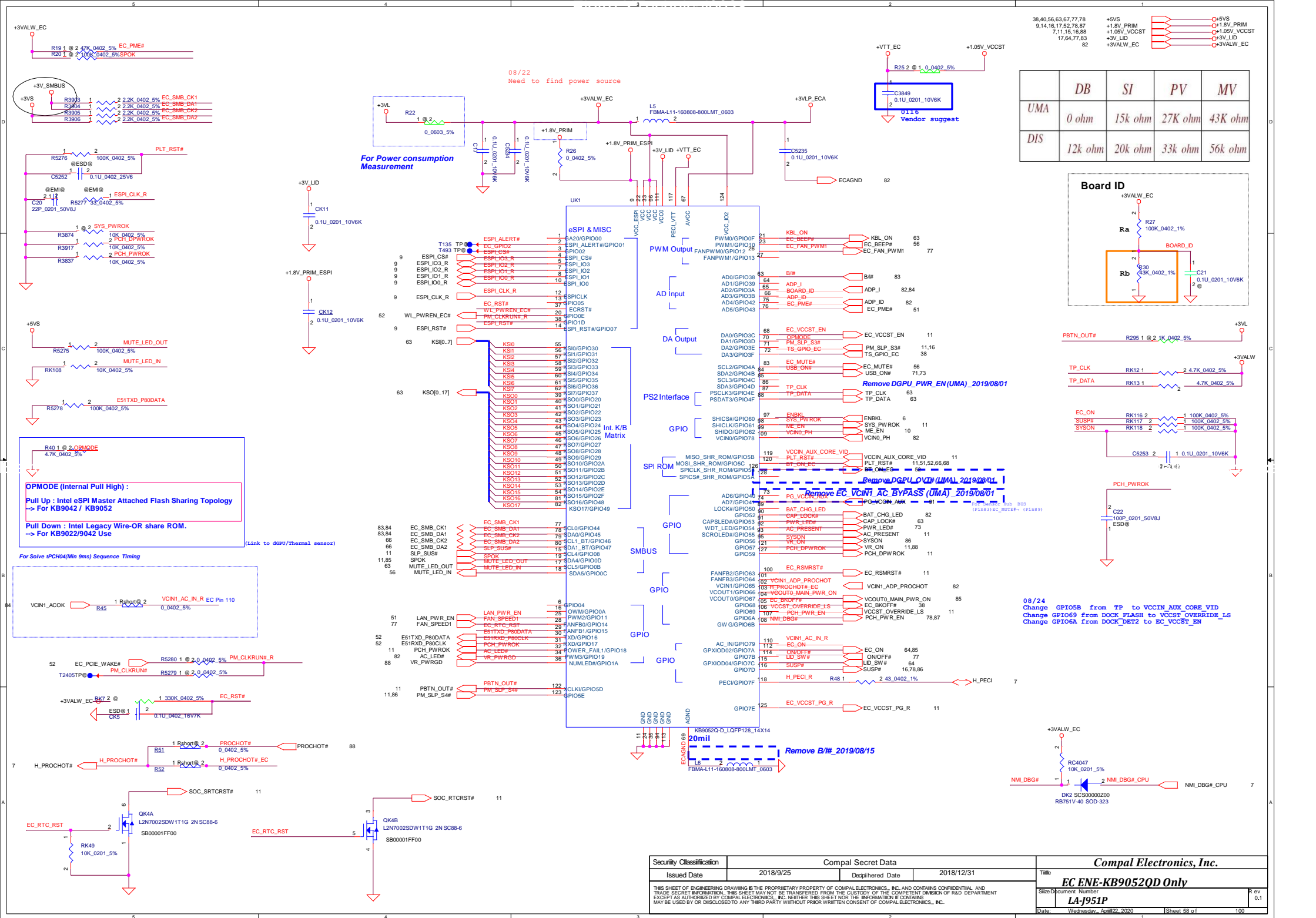


1/20-Swap DA3

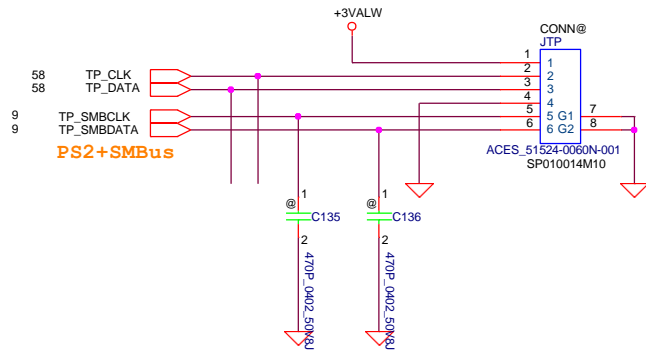


Close to Codec pin34

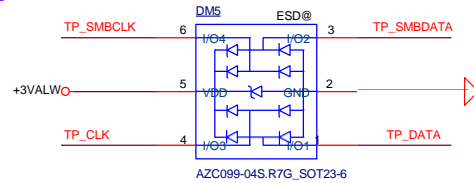




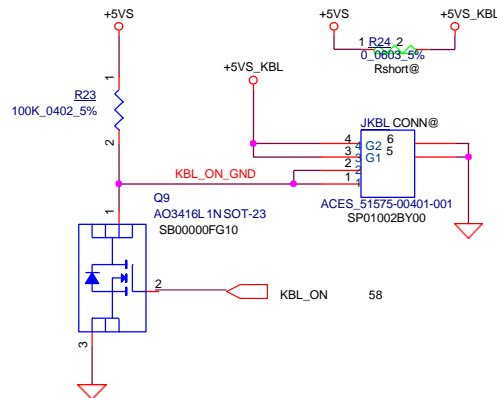
TP Button BD Connector



1st:SCA00000700, S ZEN ROW PESD5V0U2BT 3P CC SOT23 ESD
2nd:SCA00000100, S ZEN ROW L30ESDL5VOC3-2 CA SOT23 ESD
3rd:SCA000001100, S ZEN ROW PIDLOC3C 3P CA SOT23
4th:SC600001600, S DIO ROW AZC199-025.R7G CC SOT23 ESD



Function Field:32.1,32.4



9,11,17,51,52,58,66,78,85,86,87,91

+3VALW

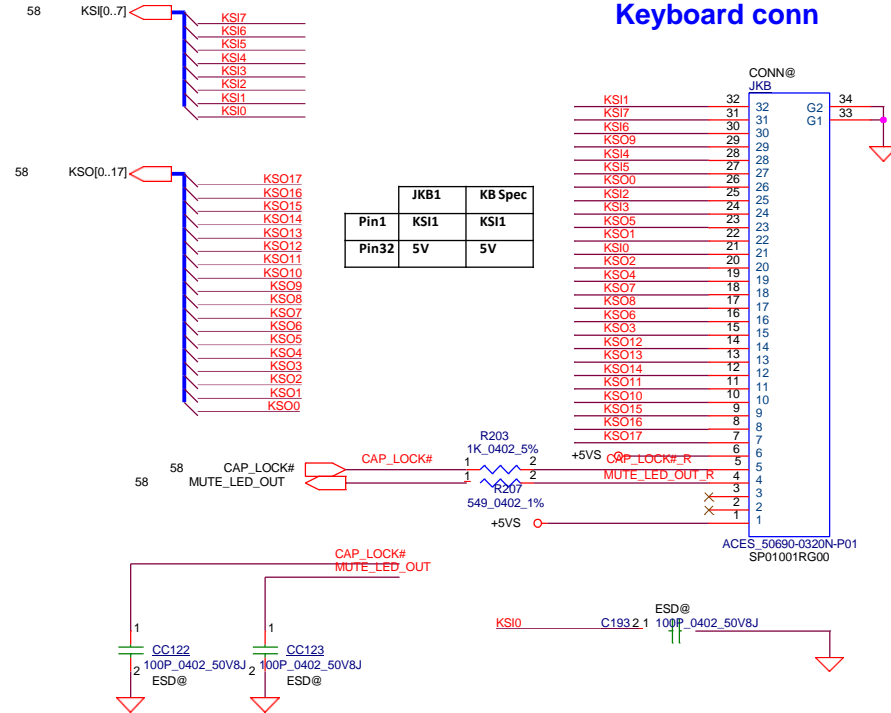
+3VALW

16,67,71,73,78,85,86,88,89,91

+5VALW

+5VALW

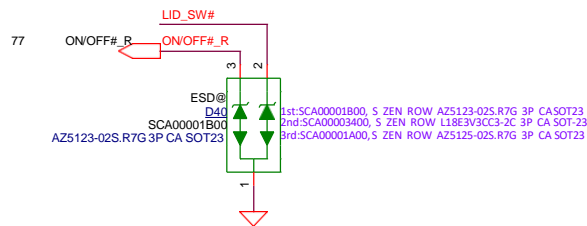
Keyboard conn



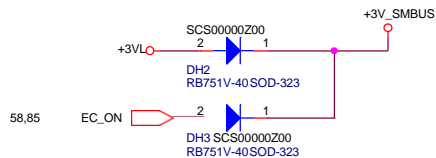
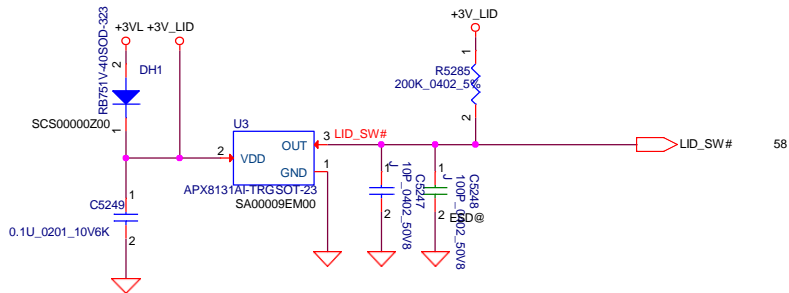
Pin1	KS11	KS11
Pin32	5V	5V

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/01/08	Deciphered Date	2020/01/08	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				KB/TP
				Size Document Number Custom LA-J951P
				Rev 0.1
				Date: Wednesday, April 22, 2020
				Sheet 63 of 100

ESD Diode

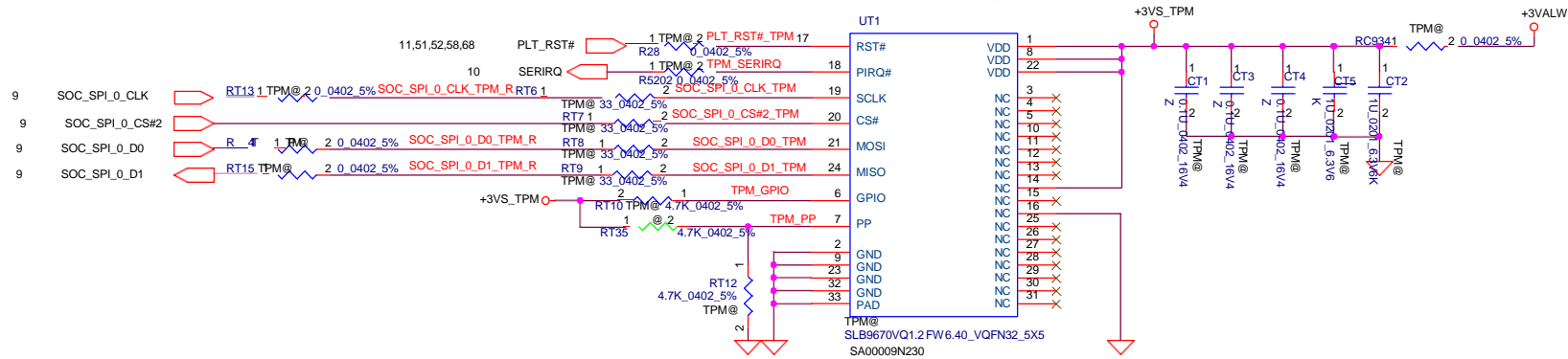


Lid Switch (Hall Effect Sensor)



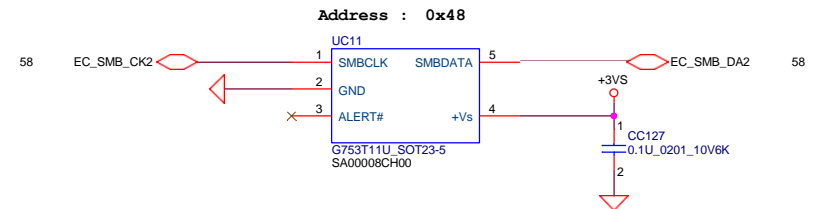
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2018/01/08		Deciphered Date		2020/01/08		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						HW Reserve			
						Size/Document Number		Rev	
						Custom		0.1	
						LA-J951P			
						Date:		Wednesday, April 22, 2020	
						Sheet		64 of 100	

TPM2.0



Finger printer

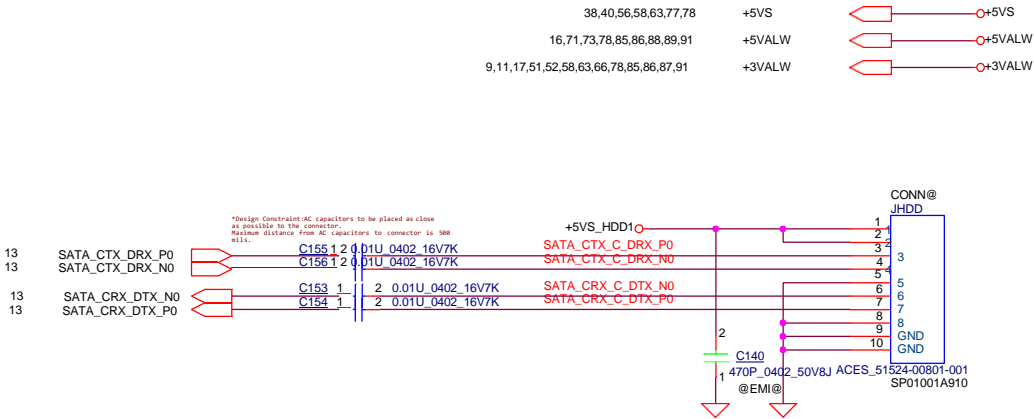
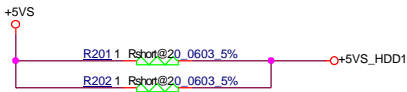
CPU THERMAL SENSOR



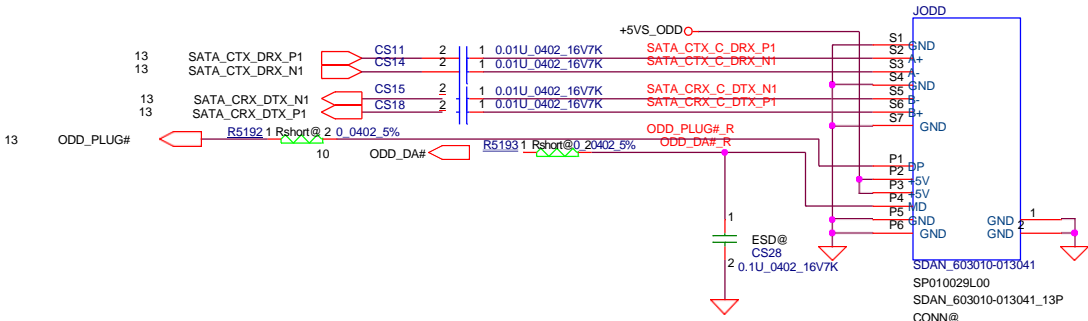
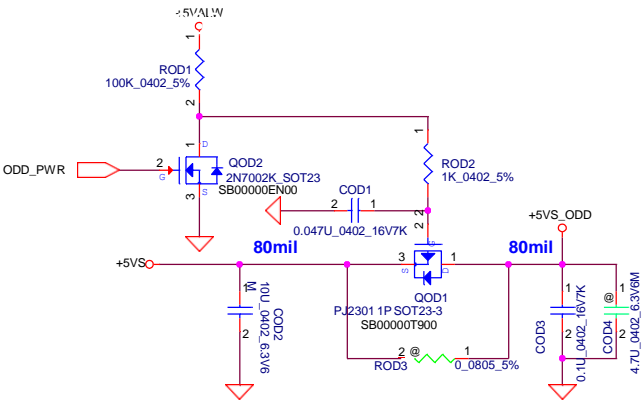
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/01/08	Deciphered Date	2020/01/08	Title	TPM/Screw
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	Rev
				LA-J951P	0.1
				Date: Wednesday, April 22, 2020	Sheet 66 of 100

2.5" SATA HDD

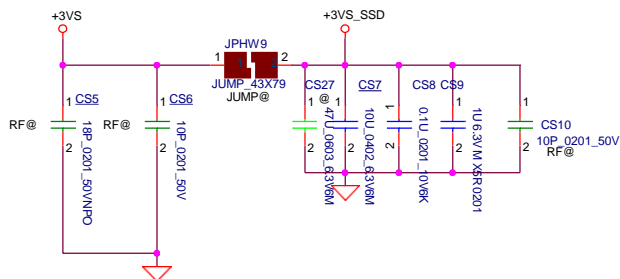
<PV> change short pad



SATA ODD



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2018/01/08	Deciphered Date	2020/01/08	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					HDD/ODD Conn	
					Size/Document Number	Rev
					Custom LA-J951P	0.1
					Date: Wednesday, April 22, 2020	
					Sheet 67 of 100	

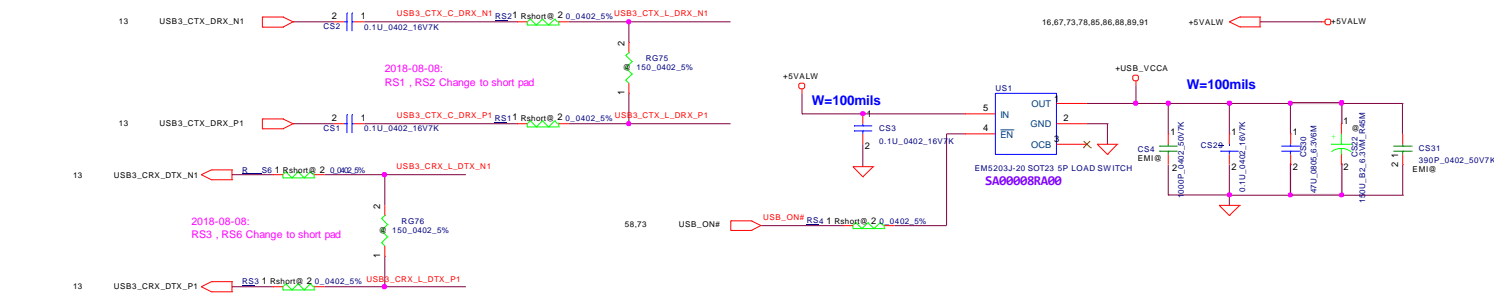


8,9,10,11,12,13,23,24,38,40,51,56,58,66,73,77,78,88

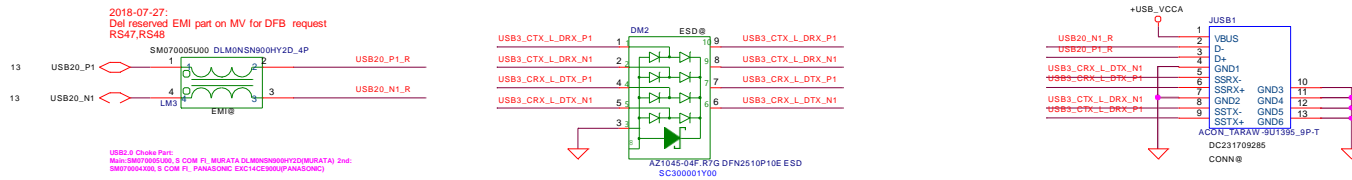
+3VS +3VS

Figure 1-2-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

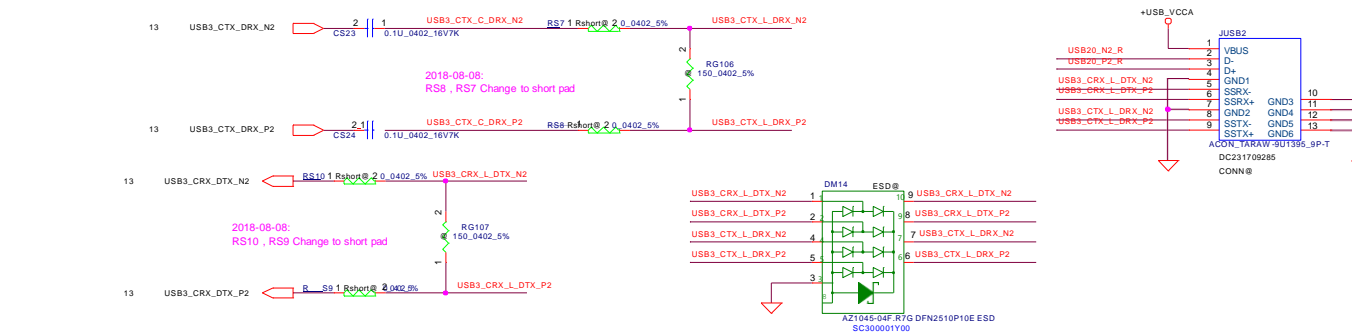
PCIe Link Details		PCIe Controller #1					PCIe Controller #2					PCIe Controller #3																					
PCIe Link ID	PCIe Link Name	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Base-U	1st LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	
	2nd LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	
	3rd LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	
	4th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	
	5th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	
	6th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	7th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	
	8th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	9th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	10th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
Premium-U	1st LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	2nd LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	3rd LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	4th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	5th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	6th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	7th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	8th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	9th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP
	10th LP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP	RP



USB2.0/USB3.0 port 1



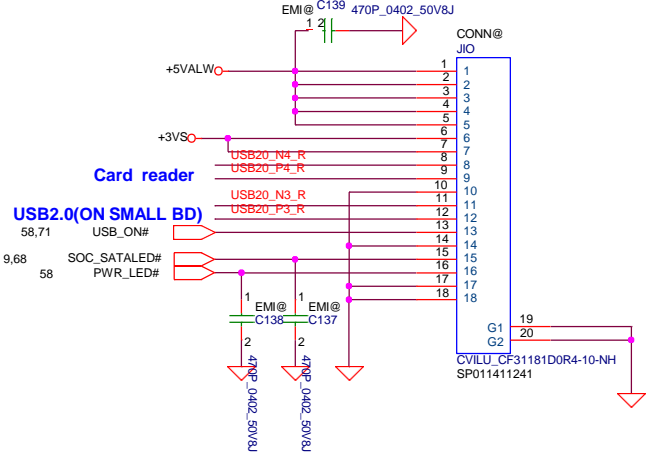
USB2.0/USB3.0 port 2



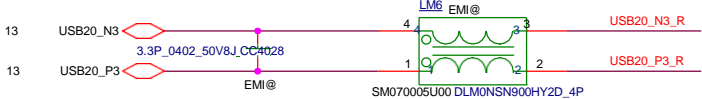
USB2.0/USB3.0 port 2



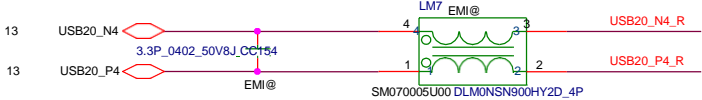
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)



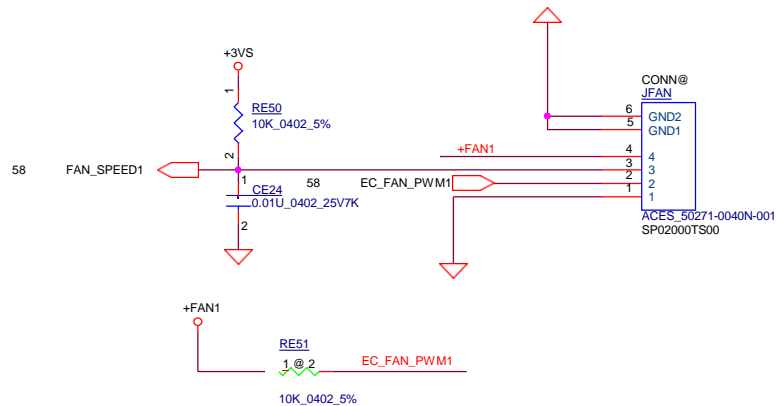
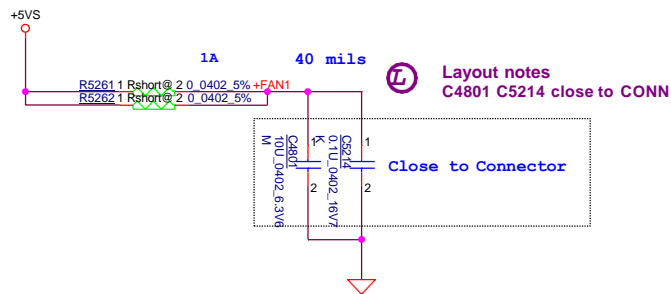
2018-07-27:
Del reserved EMI part on MV for DFB request
RS51,RS52,RS53,RS54



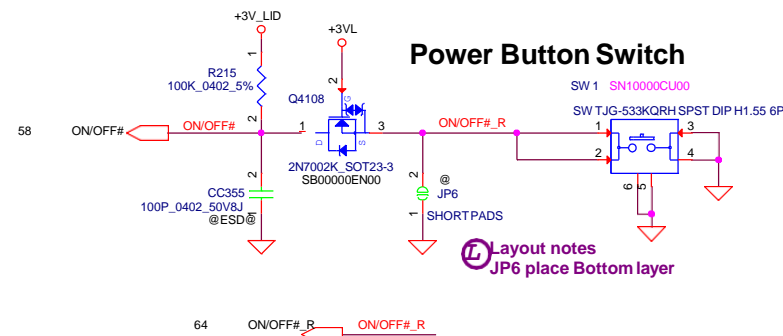
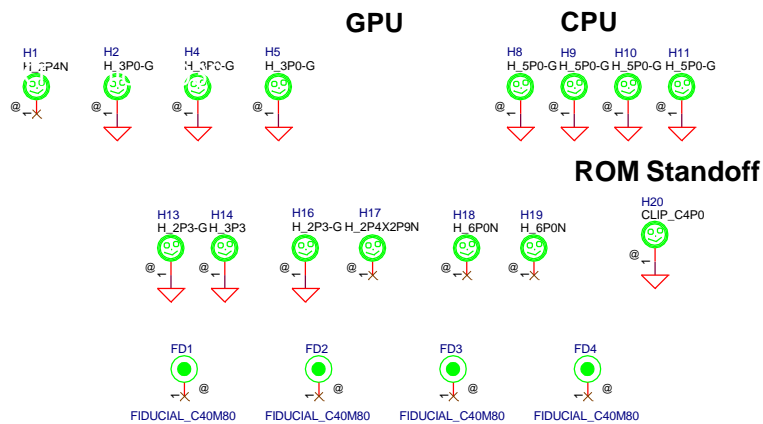
2018-07-27:
Del reserved EMI part on MV for DFB request
RS51,RS52,RS53,RS54



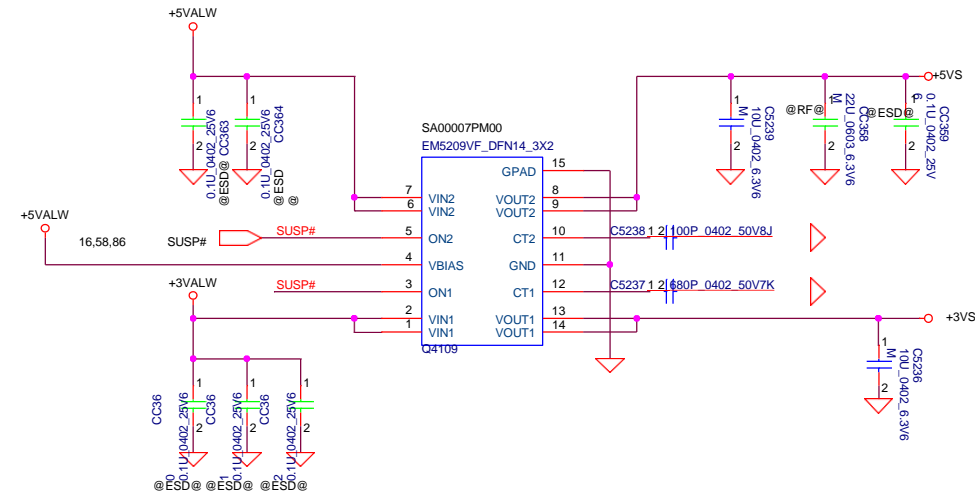
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/01/08	Deciphered Date	2020/01/08	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HW Reserve	
Size		Document Number		Rev	
Custom		LA-J951P		0.1	
Date:		Wednesday, April 22, 2020		Sheet	73 of 100



Screw Hole



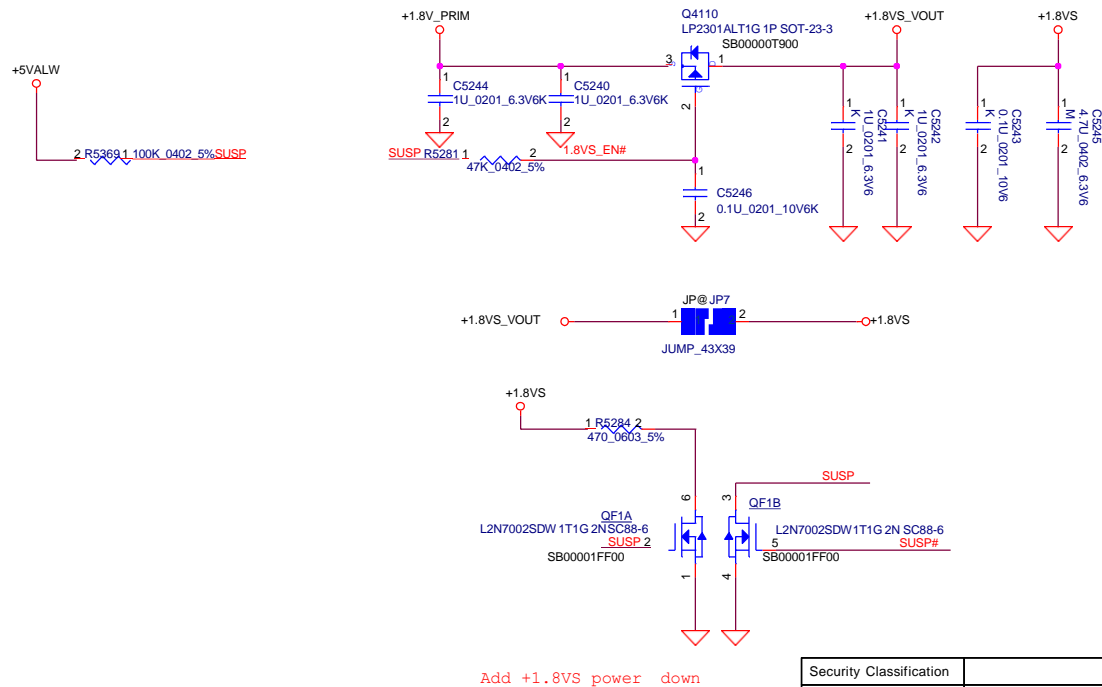
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/01/08	Deciphered Date	2020/01/08	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				FAN	
Size/Document Number		Custom		Rev	
LA-J951P				0.1	
Date:		Wednesday, April 22, 2020		Sheet	
				77 of 100	



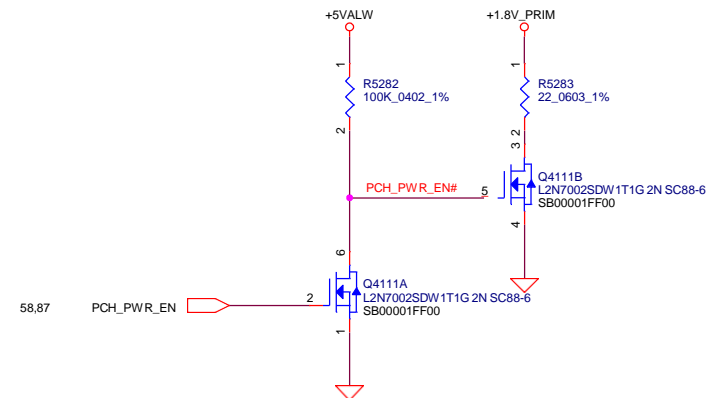
+3VS 8,9,10,11,12,13,23,24,38,40,51,56,58,66,68,73,77,88
+5VS 38,40,56,58,63,67,77

+1.8V_PRIM TO +1.8VS

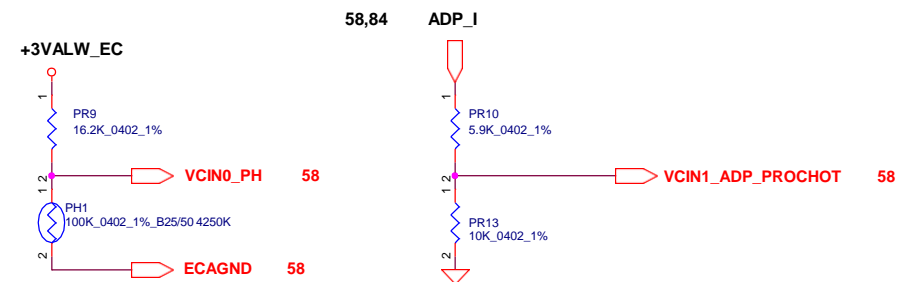
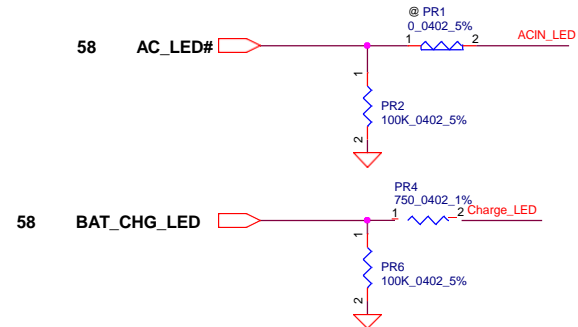
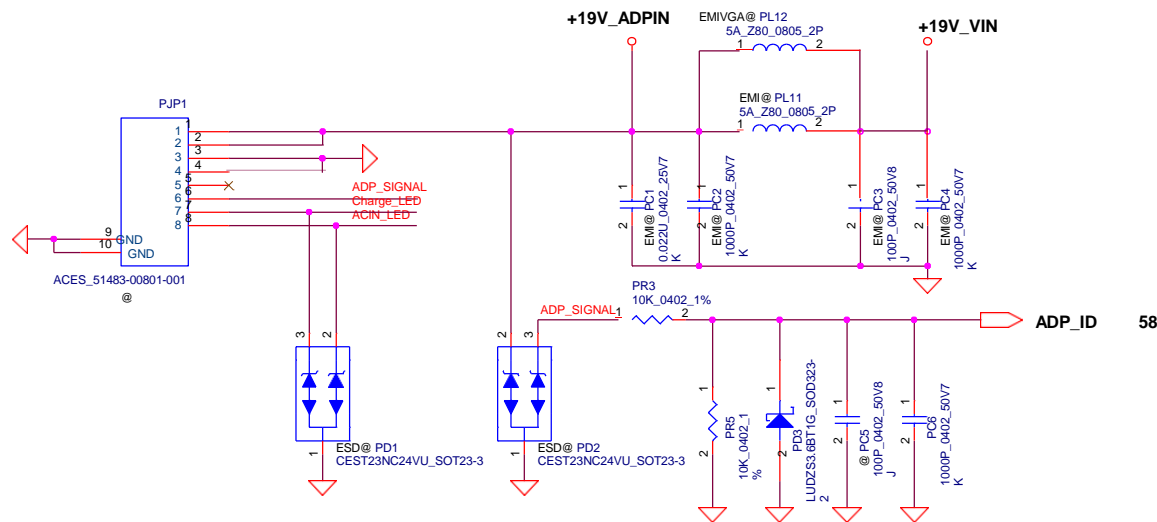
I (Max) : 0.2 A (Codec)
RDS (max) : 150 mohm
V drop : 0.03V



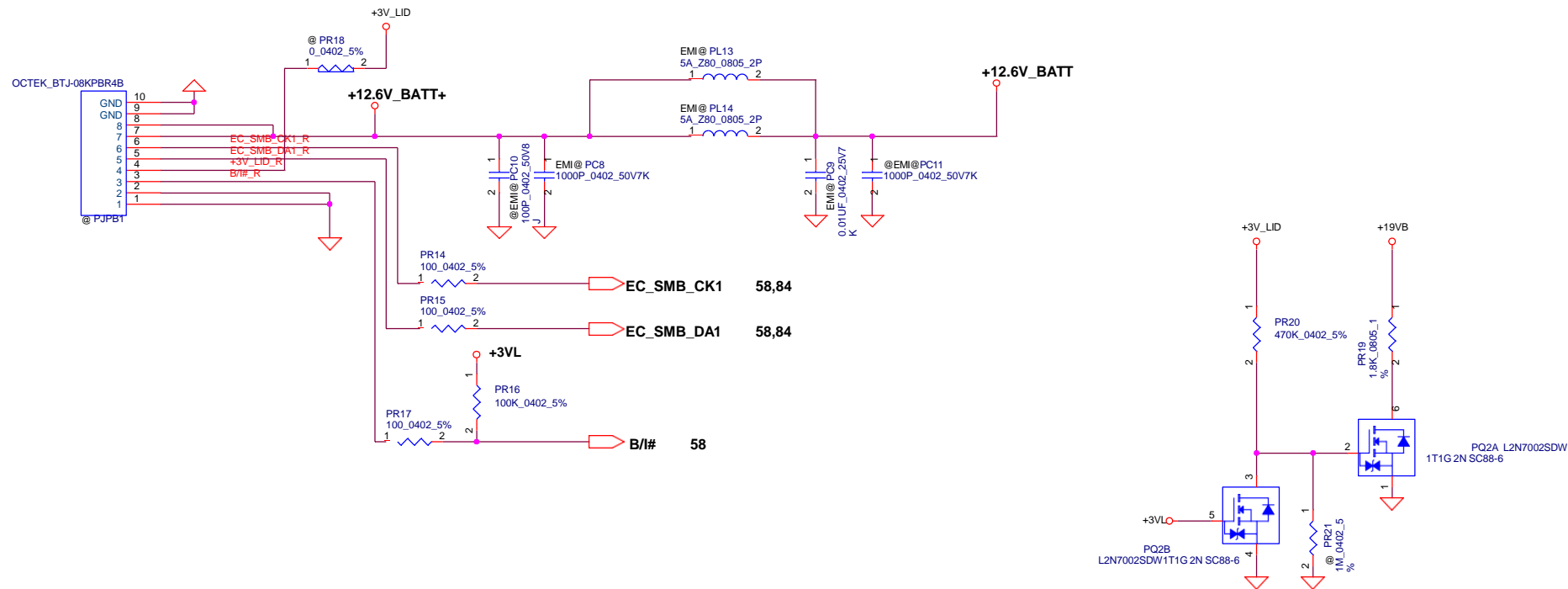
For +1.8V_PRIM Discharge



Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2018/01/08		Deciphered Date		2020/01/08		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						DC Interface			
						Size/Document Number		Rev	
						Custom LA-J951P		0.1	
						Date: Wednesday, April 22, 2020			
						Sheet 78		of 100	

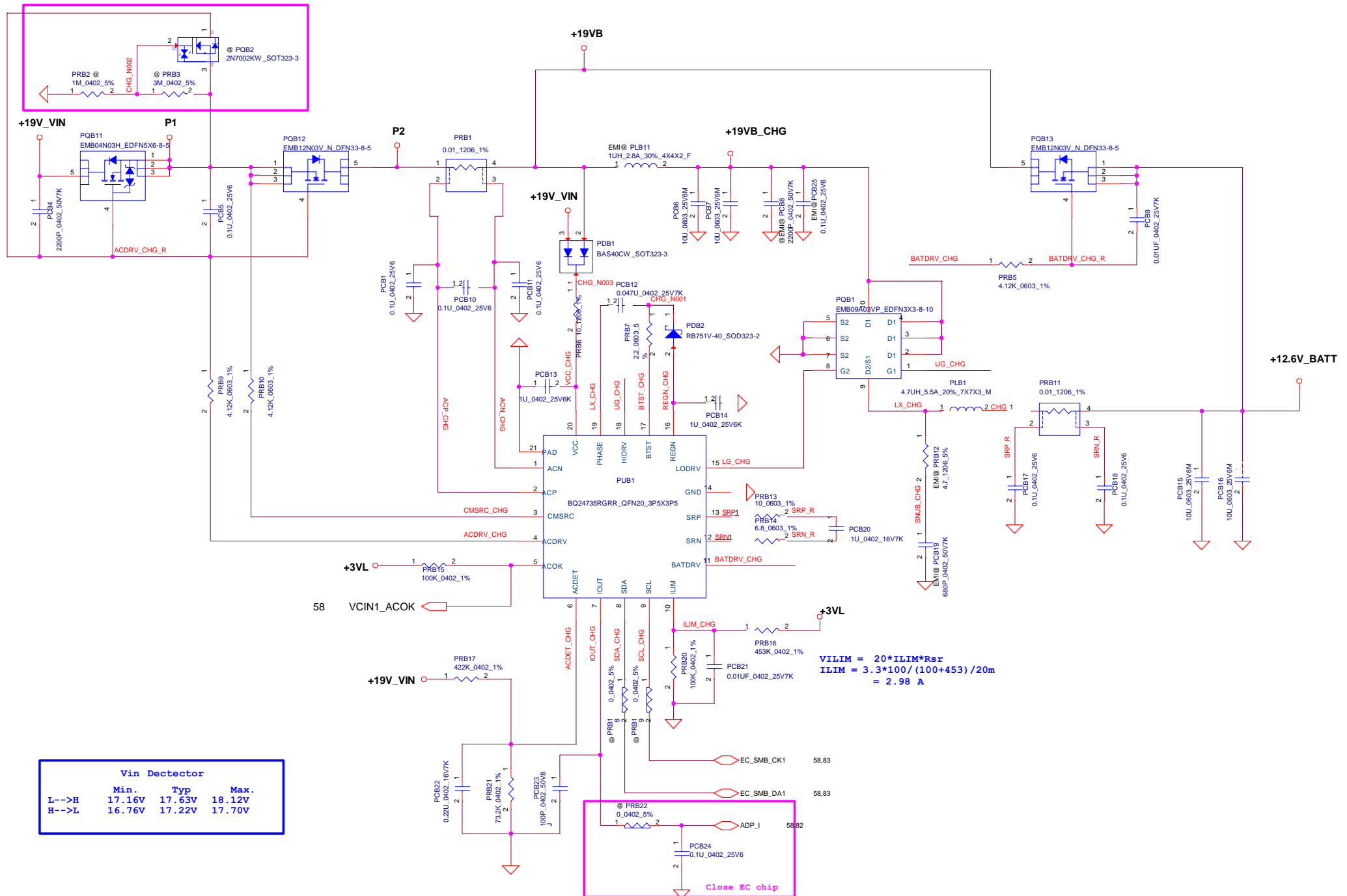


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/10/15	Deciphered Date	2021/10/15	Title	DC Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	Rev
				GPI50	0.1
				Date: Wednesday, April 22, 2020	Sheet 82 of 100



Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2019/10/15	Deciphered Date	2021/10/15		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				BATT Conn		Rev 0.1			
				Size/Document Number					
				GPI50					
				Date:					
				Wednesday, April 22, 2020					
				Sheet		83		of 100	

Protection for reverse input



Vin Detector

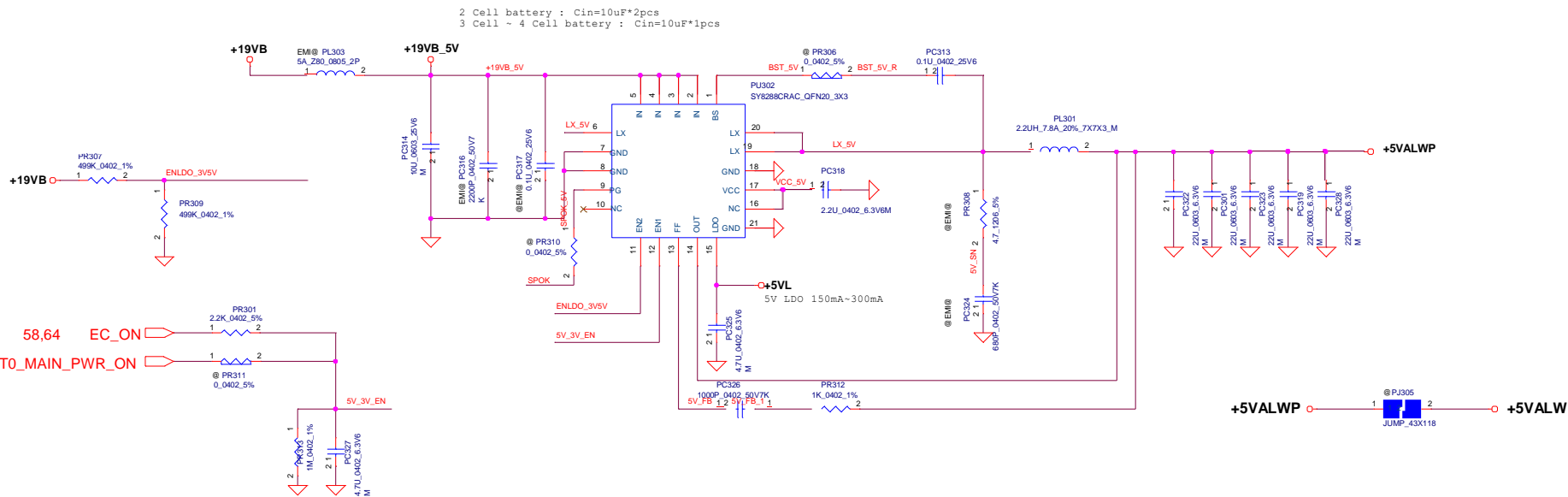
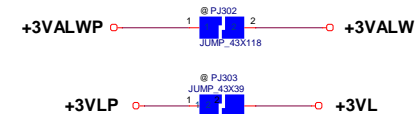
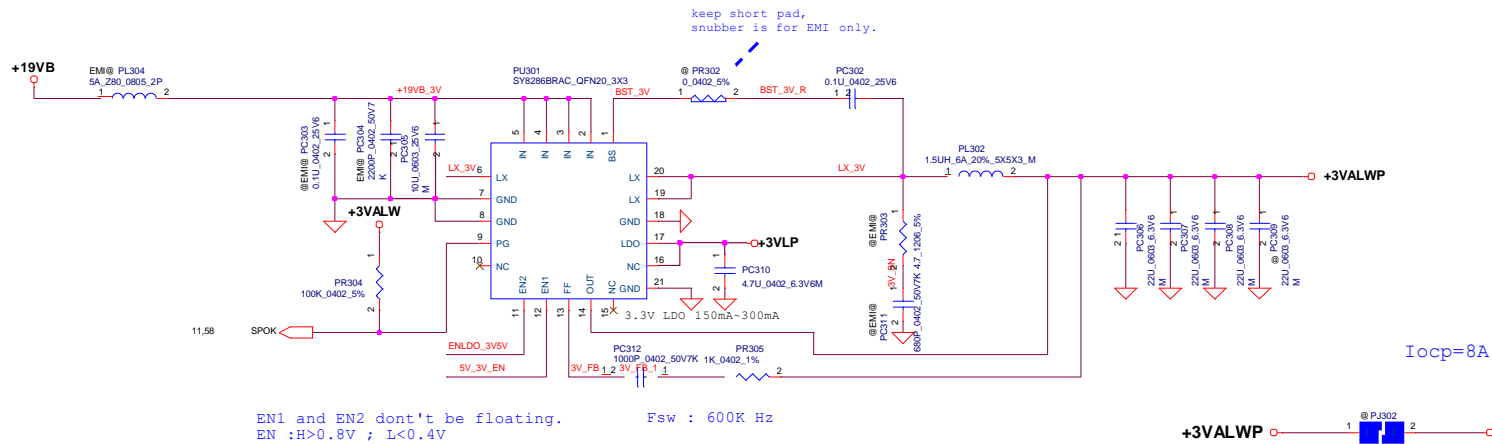
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$$V_{ILIM} = 20 \cdot ILIM \cdot R_{sr}$$

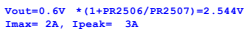
$$ILIM = \frac{3.3 \cdot 100}{(100 + 453)} / 20m$$

$$= 2.98 A$$

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2019/10/15	Deciphered Date	2021/10/15	Title	CHARGER
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Size Document Number
					Rev 0.1
Date: Wednesday, April 22, 2020					Sheet 84 of 100

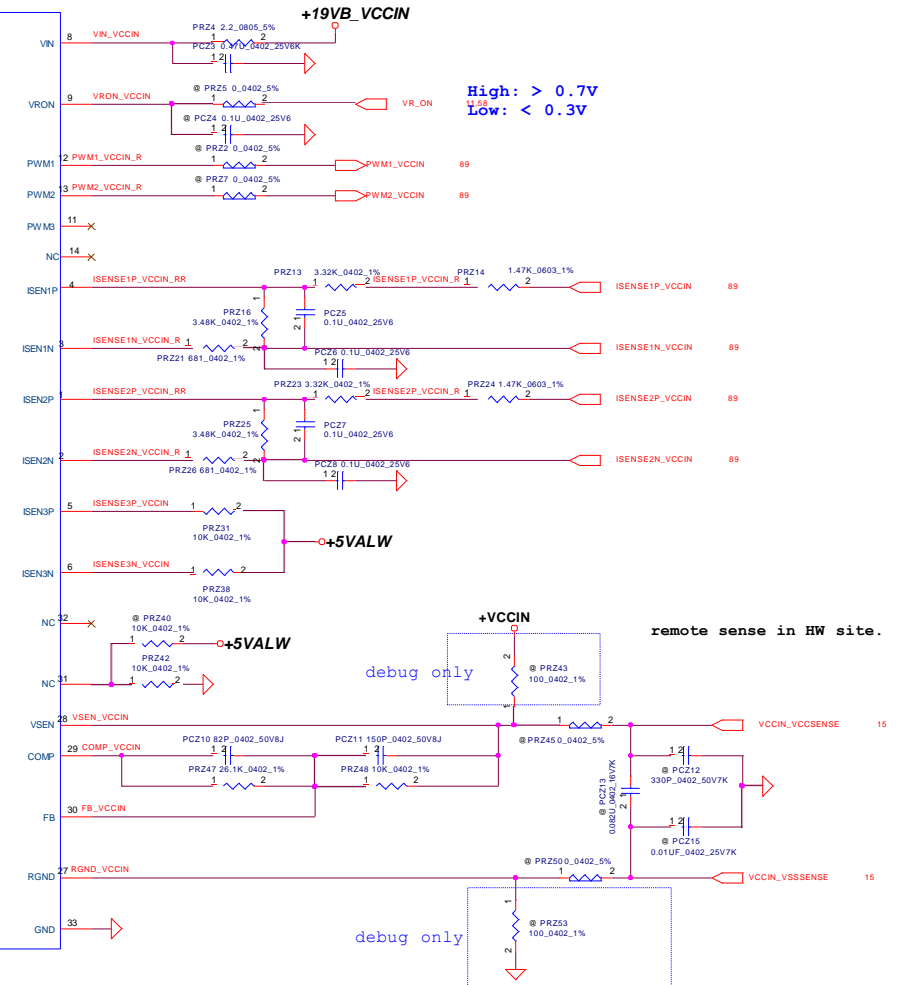
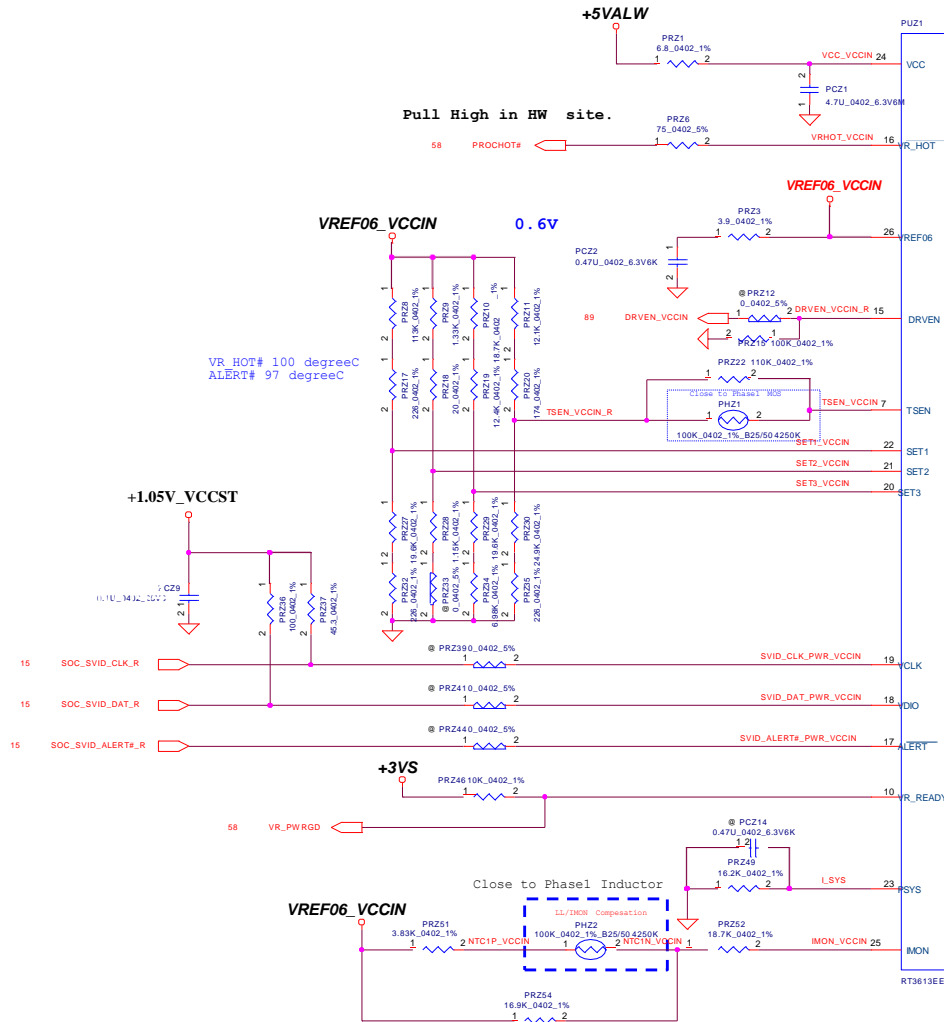


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2019/10/15	Deciphered Date	2021/10/15	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	Rev
				Custom	0.1
				Date: Wednesday, April 22, 2020	Sheet 85 of 100



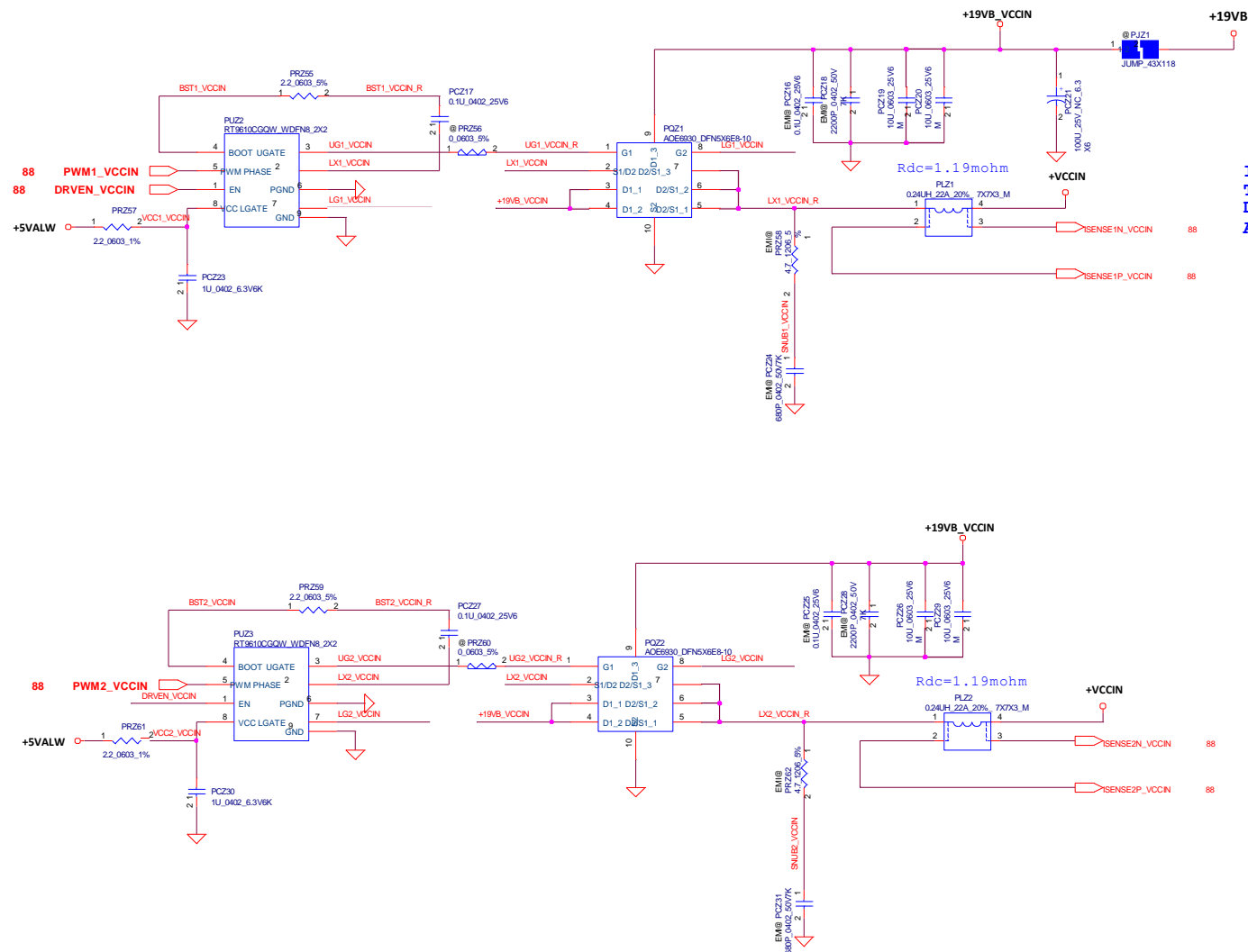
Secrecy Classification	Compall Secrete Data		Compal Electronics, Inc.	
Issued Date	2/19/10/15	Declassified Date	2/19/10/15	Title 1.2VP/0.6VSP/2.5V
THIS SHEET OF DRAWINGS ORIGINATES FROM THE PROPERTY OF COMPAL ELECTRONICS U.S. AND CONTAINS CONFIDENTIAL TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT CUSTOMER AND DEPARTMENT SECRETARY. ANY DISCLOSURE OF THIS SHEET MAY BE SUBJECT TO THE PENALTIES OF THE TRADE SECRET ACT. INFORMATION RECEIVED AND BEING USED OF DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.			Doc. Control Number CL181	
Date: 04/04/2022			Drawn By: P-00	

RT3613EEGQW-02 is not MP part



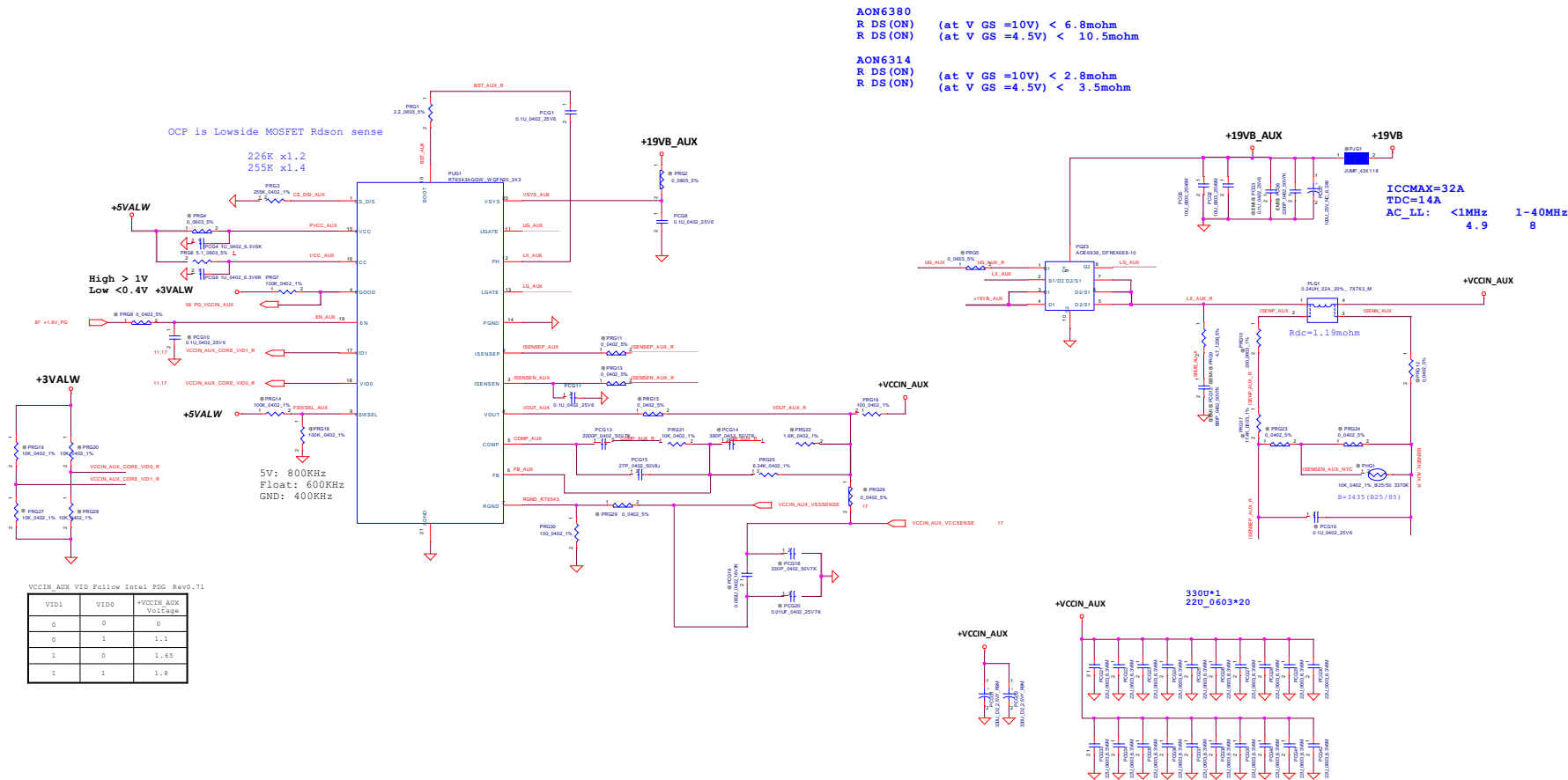
31 pin is a function to fix decay down slew rate to reduce acoustic noise.
High(5V): enable
Low(0V): disable
this pin can dynamic change state.

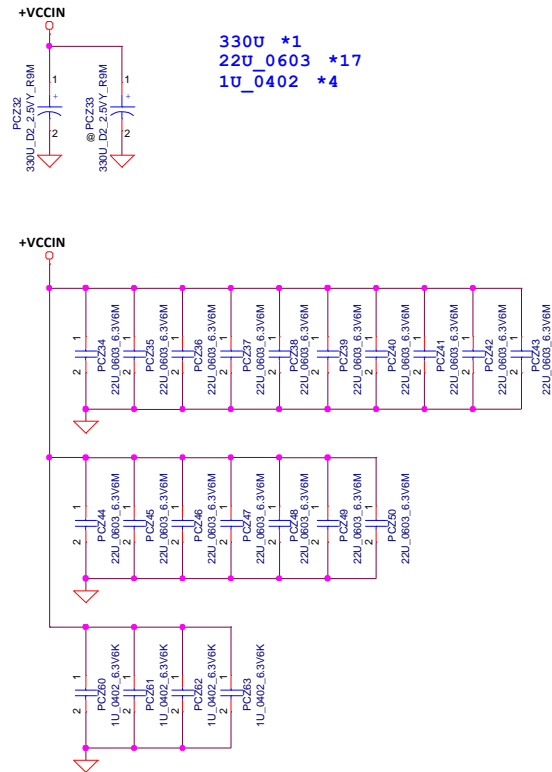
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2019/10/15	Deciphered Date	2021/10/15	CPU_CORE	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DEPARTMENT OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Sheet Number	Rev
				GPI50	2.1
				Date: Wednesday, April 22, 2020	Sheet 89 of 100



ICCMAX=55A
TDC=30A
DC_LL=2mohm
AC_LL=4.2mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/10/15	Deciphered Date	2021/10/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
CPU Power stage				Rev 0.1
Size Document Number				GP150
Date: Wednesday, April 22, 2020				Sheet 89 of 100





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/10/15	Deciphered Date	2021/10/15	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR DECOUPLING	
				Size Document Number	Rev
				GPI50	0.1
				Date	Wednesday, April 22, 2020
				Sheet	90 of 100

